Reg. No. | | | | | | | | | | | | |

Question Paper Code : 60444

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 – DIGITAL ELECTRONICS

(Regulations 2008/2010)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester – ECE – Regulations 2009)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Simplify the following expression using Boolean laws.

   $Y = AB + AB' - A'C - A'C'$.

2. Compare the performance of TTL and CMOS devices in terms of power dissipation per gate and noise margin.

3. Draw full adder circuit using only NAND gates.

4. Distinguish between decoder and demultiplexer.

5. State the status of the JK flip flop if suppose the setup and holding time is not met.

6. List the advantage and disadvantages of ripple counters.

7. What is the size of the decoder in an 8 × 4 ROM?

8. Comment whether is it possible to share the product terms between different outputs in a PLA.

9. How an ASM chart is different from the conventional flow chart?

10. How to eliminate the hazards that could occur in the asynchronous sequential circuits?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Reduce the following expression in SOP and POS forms using Karnaugh map.

$f = \sum m(0,2,3,10,11,12, 13,16,17, 18, 19, 20, 21, 26, 27)$. (10)

(ii) Simplify the following function and implement them with two-level NAND gate circuits. (6)

$F(A,B,C,D) = A'B'C + AC + ACD + ACD' + A'B'D' + B'CD$.

Or

(b) (i) Obtain the minimal expression using the tabular method and implement it in universal logic. (10)

ΠM (6, 7, 8, 9). d(10, 11, 12, 13, 14, 15)

(ii) Prove that two open – collector TTL inverters, when connected together produce the NOR function. (6)

12. (a) (i) Design a combinational circuit with three inputs and one output with following criteria. (8)

(1) The output is 1 when the binary value of the inputs is less than or equal to 3. The output is 0 otherwise.

(2) The output is 1 when the binary value of the inputs is an odd number.

(3) The output is 1 when the binary value of the inputs is an even number.

(ii) Implement a full adder with a decoder and NAND gates. The adder inputs are A, B and C. The adder produces outputs S and C_0. (8)

Or

(b) (i) Design an excess-3-code to BCD using the unused combinations of the code as don't-care conditions. (10)

(ii) Implement the following function with a multiplexer. (6)

$F(A, B, C, D) = \sum (0, 2, 5, 7, 11, 14)$

13. (a) Using JK flip flop, design a counter that goes through states 3,4,6,7 and 3 .... Is the counter self starting? Modify the circuit such that whenever it goes to an invalid state it comes back to state 3. (16)

Or

(b) (i) Analyze the operation of serial in parallel out and parallel in and parallel out using D flip flop. (8)

(ii) Draw the state diagram and state table for a 4 bit odd parity generator. (8)

14. (a) (i) Show how the memory cycle timing waveforms for the write and read operations. Assume a CPU clock of 50 MHz and a memory cycle time of 50ns.

(ii) Realize two outputs F_1 and F_2 using a 4 × 2 PROM. (16)

$F_2 = \sum m(0,4,7)$

$F_2 = \sum m(1,3,6)$

$F_3 = \sum m(1,2,4,6)$

Or

(b) (i) Realize the following functions using a PAL with four inputs and 3-wide AND-OR structure. Also write the PAL programming table. (8)

$F_1(A, B, C, D) = \sum m(6, 8, 9, 12, 13, 14, 15)$

$F_2(A, B, C, D) = \sum m(1,4,5,6,7,10, 11,12,13)$

$F_3(A, B, C, D) = \sum m(4, 5, 6, 7, 10, 11)$

$F_4(A, B, C, D) = \sum m(4, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15)$

(ii) With the neat sketch, discuss the architecture of FPGA. (8)

15. (a) Draw the state diagram, state table and ASM chart for a 2 bit binary counter having one enable line E such that E = 1 counting enabled and E = 0 counting disabled. (16)

Or

(b) (i) Write a verilog code for BCD up/down counter using SR flip flop. (8)

(ii) Write a verilog code for 4 bit ripple adder using half subtractors. (8)

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