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Question Paper Code : 60537

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Sixth Semester

Electronics and Instrumentation Engineering

EI 2353/EI 63/10133 EI 603 — DIGITAL SYSTEM DESIGN

(Regulations 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Which logic family performs better in a high-noise environment : CMOS or TTL? Why?

2. What is the main advantage of ECL over other IC technologies? In what type of application should ECL not be considered?

3. List two major differences between PAL and PEA.

4. What does PAL10L8 specify?

5. Differentiate volatile and non-volatile memory.

6. What is memory expansion?

7. What does the terms SPAN and offset mean with reference to ADC?

8. What is the basic difference between Time and frequency measurement?

9. Give two valid reasons that justify the need for testing of digital circuits.

10. Define the term controllability and observability with respect to design for testing of logic circuits.

PART B — (5 × 16 = 80 marks)

11. (a) Design a full adder using CMOS and dynamic CMOS. Also discuss their performances in detail.

Or

(b) With a neat sketch explain the

(i) TTL to CMOS

(ii) CMOS to TTL interfacing.

12. (a) How does a PLA differ form PAL? Implement the following functions using Read Only Memory (ROM)

$W(A,B,C,D) = \Sigma m(3,7,8,9,11,15)$

$X(A,B,C,D) = \Sigma m(3,4,5,7,10,14,15)$

$Y(A,B,C,D) = \Sigma m(1,5,7,11,15)$.

Or

(b) Realize the sum of product expression $Y = \Sigma m(0,5,10,15)$ using 4:1 multiplexers.

13. (a) (i) Discuss on the design of 64 × 64 memory. (8)

(ii) Show how two 16 × 4 memory can be connected to implement 16 × 8 memory. (4)

(iii) Comment on programming of ROMs. (4)

Or

(b) (i) Demonstrate with a timing diagram, the access time of PROM. (4)

(ii) How many address lines are required for a memory that has following number of bits?

(1) 1024

(2) 4098

(3) 256

(4) 16,384. (4)

(iii) With a typical three-transistor DRAM cell explain the Read and write operation with timing diagram. (8)

14. (a) With a neat functional diagram, explain four decimal digit multiplexed display.

Or

(b) With a neat functional diagram, explain the operation of frequency counter.

15. (a) Explain the concept of generic boundary scan in detail.

Or

(b) Explain any one of the system level design for test approach in detail.
