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**Question Paper Code : 60529**

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Fourth Semester

Electronics and Instrumentation Engineering

EI 2253/EI 43/10133 EE 406/080300014 — DIGITAL LOGIC CIRCUITS

(Regulations 2008/2010)

(Common to PTEI 2253/10133 EE 406 – Digital Logic Circuits for B.E. (Part-Time) Second Semester – EEE – Regulations 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are cyclic codes?

2. Simplify the function $Y = \Sigma m(1,3,5,7)$.

3. Implement the following functions using NOR gates

   (a) NOT gate

   (b) Ex-OR gate.

4. State the difference between a decoder and a demultiplexer.

5. How could you change an edge-triggered RS flip-flop into an edge-triggered JK flip-flop?

6. What is a ring counter?

7. What is meant by fusible link? How many types of fuse technologies are used in PROM?

8. Draw the logic circuit for CMOS NAND gate.

9. What is memory expansion?

10. Define cycle in asynchronous circuits.

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the given Boolean function using K-Map.

(i) $F(A,B,C,D) = \Sigma m(1,2,3,5,7,9,10,11,13,15)$. (8)

(ii) $F(W,X,Y,Z) = W'X'Y + WZ + XZ' + YZ' + WY' + W'X'$. (8)

Or

(b) Using Quine McCluskey method, simplify the given function.

$F(A,B,C,D) = \Sigma m(2,3,7,9,11,13) + \Sigma d(1,10,15)$. (16)

12. (a) (i) Implement the following Boolean function using suitable muliplexer $F(A,B,C) = \Sigma m(1,3,5,6)$. (8)

(ii) Design a full subtractor with half subtractors. (8)

Or

(b) (i) Design a code converter for BCD to gray code conversion. (10)

(ii) Explain how the demultiplexer used as a decoder. (6)

13. (a) Design a synchronous MOD – 10 down counter using J-K flip-flops. (16)

Or

(b) (i) Describe the parallel in – serial out shift register with neat logic diagram. (8)

(ii) Explain the function of J-K flip-flop using a suitable diagram and discuss how does it differ from S-R flip-flop. (8)

14. (a) With a suitable example, explain the analysis of asynchronous sequential circuit. (16)

Or

(b) Design a sequence detector to detect the sequence 11010. (16)

15. (a) (i) Design a BCD to Excess – 3 code converter and implement using suitable PLA. (10)

(ii) Give the classification of semiconductor memory. (6)

Or

(b) (i) Draw and explain the circuit for tri-state TTL inverter. (10)

(ii) Give the characteristics of ECL family. (6)

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