Reg. No.: | | | | | | | | | | | | |

Question Paper Code : 60376

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Third Semester

Computer Science and Engineering

CS 2202/CS 34/EC 1206 A/10144 CS 303/080230012 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2008/2010)

(Common to PTCS 2202 – Digital Principles and System Design for B.E. (Part-Time) Second Semester – CSE – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(101101.1101)_2$ to decimal and hexadecimal form.
2. What are the limitations of Karnaugh map?
3. What is the drawback of serial adder? For which applications are they preferred?
4. Distinguish between half adder and full adder.
5. Draw the truth table and circuit diagram of 4 to 2 encoder.
6. Distinguish EEPROM and flash memory.
7. List any two mechanisms to achieve edge triggering of flip flops.
8. What is a ring counter?
9. What is an implementation table?
10. Write short notes on Static-1 hazard.

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the following Boolean function using Quine-McClusky method $F=(A,B,C,D,E)=\Sigma m(0,1,3,7,13,14,21,26,28)+\Sigma d(2,5,9,11,17,24)$. (16)

Or

(b) (i) Simplify the given Boolean function in POS form using K-map and draw the logic diagram using only NOR gates.

$F=(A,B,C,D)=\pi M(0,1,4,7,8,10,12,15)+d(2,6,11,14)$ (10)

(ii) Convert 78.5_{10} into binary. (3)

(iii) Find the dual and complement of the following Boolean expression. $xyz'+x'yz+z(xy+w)$. (3)

12. (a) Design a full adder using 2 half adders.

Or

(b) Design a combinational circuit to convert binary to gray code.

13. (a) (i) Write notes on PLA and PAL. (8)

(ii) Implement $F = (A, B, C, D) = \Sigma(1,3,4,11,12,13,14,15)$ using 8×1 multiplexer. (8)

Or

(b) (i) Write notes on RAM, its operations and its types. (10)

(ii) Design a 4 - input priority encoder. (6)

14. (a) A clocked sequential circuit is provided with a single input x and a single output z. Whenever the input produces a string of pulses 111 or 000 and at the end of the sequence it produces an output z = 1 and overlapping is not allowed. (16)

(i) Obtain the state diagram

(ii) Obtain the state table

(iii) Design the sequence detector.

Or

(b) Using D flip-flops, design a synchronous counter, to count the following repeated binary sequence 0,1,2,4,6. Write the VHDL code for the same. (16)

15. (a) Design an asynchronous sequential circuit with two input x and y and with one output z whenever y is 1, input x is transferred to z. when y is 0, the output does not change for any change in x. (16)

Or

(b) (i) Define: Hazards. (2)

(ii) Explain about:

(1) Static Hazards (5)

(2) Dynamic Hazards (5)

(3) Essential Hazards. (4)
