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Question Paper Code : 60393

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Sixth Semester

Computer Science and Engineering

CS 2354/CS 64/10144 CS 604 — ADVANCED COMPUTER ARCHITECTURE

(Regulations 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is named dependence?
2. Prediction accuracy is 80% (for instruction in the buffer). Hit rate in the buffer is 90% (for branch prediction taken). Compute the branch penalty.
3. Differentiate between VLIW and EPIC Processors.
4. Write about the Register Stack Mechanism in IA-64 Register model.
5. What are the advantages of MIMD multiprocessors?
6. What is the importance of memory consistency model?
7. What is cache miss and cache hit?
8. What is the bus master?
9. What is meant by simultaneous multithreading?
10. What are the advantages of CMP architectures?

PART B — (5 × 16 = 80 marks)

11. (a) (i) With a neat diagram explain the Tomasulo-based processor. (10)

(ii) Briefly explain the dynamic branch prediction techniques. (6)

Or

(b) (i) Consider the following code and assume that the multiply instruction has a latency of 5, the divide instruction a latency of 10 and the add instruction latency is 2. Also assume that there are separate functional units for effective address calculations, for ALU operations, and for branch condition evaluation. For a Speculative processor, create a table showing when each instruction issues, executes, write the result and commits, for one iteration of the loop and for atleast two instructions from the second iteration. Assume one CDB and that only one instruction can commit per cycle. (10)

Loop : LD F_0, 0(R_1)

LD F_4, 0(R_2)

ADD F_0, F_0, F_2

MUL F_4, F_4, F_2

DIV F_0, F_0, F_4

SD 0(R_2), F_0

ADDI R_1, R_1, #8

ADDI R_2, R_2, #8

SUBI R_3, R_3, #1

BNEZ R_3, loop.

(ii) Discuss the basic compiler techniques for exposing ILP. (6)

12. (a) Discuss about Itanium processor and its IA 64 Instruction Set architecture.

Or

(b) What is speculative execution? Compare and contrast hardware and software speculation mechanisms.

13. (a) Discuss about the different models for memory consistency.

Or

(b) Define synchronization and explain the different mechanisms employed for synchronization among processors.

14. (a) (i) Explain the various hit time reduction techniques (8)

(ii) Explain the RAID architecture in detail. (8)

Or

(b) What are the categories of cache misses? Explain the various techniques available for reducing cache miss rate. (16)

15. (a) (i) Describe various techniques for hardware multithreading in detail. (8)

(ii) Explain single chip multiprocessor architecture with the help of diagram. (8)

Or

(b) Discuss about the major challenges and issues in the design of multi-core architectures. (16)

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