LIB
17/11/16 AN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 60381

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Fourth Semester

Computer Science and Engineering

CS 2253/CS 43/CS 1252 A/080250011/10144 CS 404 — COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulations 2008/2010)

(Also Common to PTCS 2253/10144 CS 404 – Computer Organisation and Architecture for B.E. (Part-Time) Third Semester – CSE – Regulations 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What do you mean by indexed addressing?

2. Write down the logical expression to detect overflow in adding n-bit numbers.

3. Define multiphase clocking.

4. Write down the sequence of operational steps for executing the instruction move R2, (R1).

5. Give an example for instruction hazard.

6. Define instruction throughput.

7. Define access time.

8. Draw a block diagram to show the connections of the memory to the processor.

9. Differentiate a subroutine and an interrupt – service – routine.

10. What do you mean by cycle stealing?

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Write a program that evaluate the expression : $A \times B + C \times D$ in a single accumulator processor. Assume that the processor has load, store, multiply and add instructions, and that all values fit in the accumulator. (6)

(ii) Multiply the following pair of signed 2's complement numbers using the booth algorithm. Assume A is the multiplicand and B is the multiplier. $A = 110101$ and $B = 011011$. (10)

Or

(b) Describe the circuit arrangement for binary division and illustrate the restoring and non-restoring division process. (16)

12. (a) Explain the basic organization of a micro programmed control unit.

Or

(b) Describe the sequence of control steps required to perform "Add(R2), R1" and "Unconditional Branch" for the single bus architecture. (16)

13. (a) (i) A pipelined processor has two branch delay slots. An optimizing compiler can fill one of these slots 85 percent of the time. What is second slot only 20 percent of the time? What is the percentage improvement in performance achieved by this optimization, assuming that 20 percent of the instructions executed are branch instructions.

(ii) Describe the dynamic branch prediction algorithm for executing branch instructions in a pipelined processor.

Or

(b) Explain the data hazards and the methods for overcoming. Illustrate with example. (16)

14. (a) (i) Draw a block diagram to show the organization of a $8M \times 32$ memory using $512k \times 8$ memory chips. (8)

(ii) A block – set – associated cache consists of a total of 64 blocks divided into 4-blocks sets. The main memory contains 4096 blocks, each consisting of 128 words. Find out how many bits are there in a main memory address. Also find out how many bits are there in each of the TAG, SET and WORD fields. (8)

Or

(b) (i) Explain the structure and modes of operation of synchronous DRAMs. (10)

(ii) Write short notes on direct-mapped cache. (6)

15. (a) What do you mean by bus arbitration? Explain the different types of arbitration with neat diagrams. (16)

Or

(b) Write short notes on :

(i) Parallel Port (8)

(ii) PCI bus. (8)
