Reg. No. : | | | | | | | | | | |

Question Paper Code: 31062

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2015.

Third Semester

Instrumentation and Control Engineering

01UIC302 – DIGITAL LOGIC CIRCUITS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. State De Morgan's theorem.
2. Show that $(X + Y' + XY)(X + Y')(X'Y) = 0$
3. How does the architecture of PLA different from PROM?
4. What are the different types of shift register?
5. Define race around condition.
6. What is Hazards? And list out its types.
7. Define primitive flow table.
8. List the characteristics of digital IC's.
9. State the important characteristics of TTL family.
10. Give the classification of logic families.

PART - B (5 x 16 = 80 Marks)

11. (a) Reduce the following using tabulation method and realize the simplified function using only $F(A, B, C, D) = \sum m(14, 12, 10, 8, 6, 4, 3, 2, 1, 0)$. (16)

Or

(b) Simplify the following function using *K* maps. $F(A, B, C, D, E) = \sum m(0, 8, 11, 12, 15) + \sum d(1, 2, 4, 7, 10, 14)$ and represent the simplified expression using NAND gates. (16)

12. (a) Design full adder circuit and full subtractor circuit using logic gates and explain it function using truth table. (16)

Or

(b) (i) Using 8 to 1 multiplexer, realize the following Boolean function $T = f(w, x, y, z) = \Sigma(1,2,4,5,7,8,9,12,13)$. (4)

(ii) Design 4 bit binary to gray code converter. (12)

13. (a) (i) With a neat diagram explain the working of a master – slave JK flip flop. State its advantages. (10)

(ii) Distinguish between synchronous and asynchronous sequential circuits. (6)

Or

(b) Using SR flip-flops, design a synchronous counter which counts in the sequence 000, 111, 101, 110, 001, 010, 000. (16)

14. (a) (i) List and explain the steps used for analyzing an asynchronous sequential circuit. (10)

(ii) When do you get the critical and non-critical races? How will you obtain race free conditions? (6)

Or

(b) Design a gated latch circuit with two inputs. *G* (gate) and *D* (data) and one output *Q*. Binary information at *D* input is transferred to *Q* when *G* is 1. *Q* will follow *D* as long as *G*=1, when *G* as 0 the information that was present at the *D* input at the time transistor occurred is retained at *Q* output. Once *G*=0, a change in *D* does not change the value of output *Q*. (16)

15. (a) (i) Draw the circuit diagram and explain the working of TTL inverter with tristate output. (8)

(ii) Explain the concept and characteristics of ECL Logic family with basic Inverter circuit. (8)

Or

(b) Write a VHDL code for a up/down counter. (16)