Reg. No. : | | | | | | | | | | |

Question Paper Code: 31036

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2015.

Third Semester

Electrical and Electronics Engineering

01UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Convert $(2234.1796875)_{10}$ to its octal.
2. State the types of TTL logic.
3. How does the look-ahead-carry adder speed up the addition process?
4. What is de-multiplexer? Mention its applications.
5. What is melay and moore circuits?
6. State the difference between shift register and counters.
7. What is a fundamental mode asynchronous sequential circuit?
8. State the difference between PLA and PAL.
9. What are the predefined VHDL operators?
10. Define test bench in VHDL model.

PART - B (5 x 16 = 80 Marks)

11. (a) What is Hamming code? Discuss how the Hamming code is used to test and correct the error in the given word using suitable example. (16)

Or

(b) (i) Realize AND gate using RTL and DTL logic. (8)

(ii) Describe the operation of emitter coupled logic circuit. (8)

12. (a) Simplify the following switching functions using Karnaugh map and design the logic circuit using basic gates and using only NAND gates.

(i) $F(A,B,C,D) = \sum(0,5,7,8,9,10,11,14,15) + \phi(1,4,13)$ (8)

(ii) $F(A, B, C, D) = \prod(0, 1, 4, 5, 6, 8, 9, 12, 13, 14)$ (8)

Or

(b) (i) Realize full subtractor using 3-line to 8-line decoder. (8)

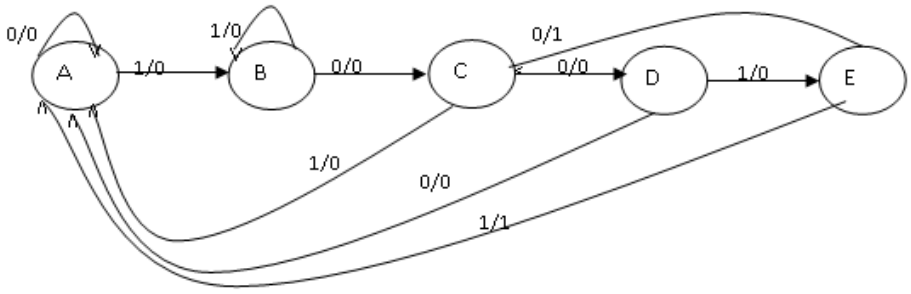
(ii) What is the need for code converters? Design a logic circuit to convert 8421 *BCD* to *XS*-3 code. (8)

13. (a) (i) Realize the JK flip flop and D flip flop using SR flip flop. (8)

(ii) Design a mod-7 counter using T flip flop. (8)

Or

(b) Design a sequential circuit using D flip flops for the state diagram given below. (16)



14. (a) (i) Obtain the primitive flow table for the asynchronous circuit that has two inputs X_2 & X_1 and one output Z. When X_1=0 the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. (10)

(ii) Discuss briefly the hazards in sequential circuits with suitable example. (6)

Or

(b) Implement the following functions using PAL:

(i) $w\ (A, B, C, D) = \sum(2, 12, 13)$ (4)

(ii) x $(A, B, C, D) = \sum(7, 8, 9, 10, 11, 12, 13, 14, 15)$ (4)

(iii) $y\ (A, B, C, D) = \sum(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$ (4)

(iv) $z\ (A, B, C, D) = \sum(1, 2, 8, 12, 13)$ (4)

15. (a) Describe about the design of sequential circuits in VHDL with an example of '*D*' flip flop in VHDL. (16)

Or

(b) Write VHDL code for the half adder circuit using (i) structural architecture (ii) data flow architecture. Assume gate delay of 5 *ns* for AND gate; 10 *ns* for XOR gate. (16)

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