Reg. No. : | | | | | | | | | | |

Question Paper Code: 31023

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2015.

Third Semester

Computer Science and Engineering

01UCS303 – COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. What is memory access time? What is the typical range of memory access time for modern RAM units?
2. Differentiate logical operations and control operations.
3. State the truth table of 2 bit binary adder.
4. List the features of booth multiplication algorithm.
5. What is meant by Data path?
6. What is operand forwarding? When it is used?
7. What is SIMD?
8. What is multithreading?
9. Define TLB hit and Miss.
10. What is meant by bus arbitration?

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Explain the basic functional units of a computer with a diagram. (8)

(ii) With a neat diagram, explain the basic operational steps needed to execute the instruction *ADD R2, (R2).* (8)

Or

(b) (i) Explain the basic operational concepts of a Computer with a neat diagram. (8)

(ii) List the addressing modes used for accessing information. Explain the usage of each of them with suitable example. (8)

12. (a) (i) What are the advantages of using carry look ahead adder? (4)

(ii) Discuss the booth's multiplication algorithm. Illustrate with the example *25 * (-16)*. (12)

Or

(b) Explain the non – restoring and restoring division algorithms. Simulate the same for *23/5*. (16)

13. (a) Explain how a data path would be modified for pipelined execution. Illustrate with the help of a neat block diagram. (16)

Or

(b) Define instruction hazard. Explain how Hazards occur due to unconditional branches? Suggest a method to avoid this hazard. (16)

14. (a) Explain concept of instruction level parallelism in detail. Discuss about the challenges. (16)

Or

(b) Discuss in detail about Flynn's classification. (16)

15. (a) What are the types of implementation in virtual memory? Explain in detail the address translation mechanism of each of them. (16)

Or

(b) Explain in detail the DMA operation and the bus arbitration. (16)