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Maximum: 100 Marks

Question Paper Code: 42272

M.E. DEGREE EXAMINATION, MAY 2015.

Second Semester

VLSI Design

14PVL202 - CAD FOR VLSI CIRCUITS

(Regulation 2014)

Duration: Three hours

Answer ALL Questions.

PART A - $(5 \times 1 = 5 \text{ Marks})$

1.	Physical design of CAD means								
	(a) Simulation	(b) Floorplanning	(c) HDL synthesis	(d) Placement					
2.	Which of the follow	lowing does not belong to placement algorithm							
	(a)Force directed	(b) Random sea	urch						
	(c) Cluster growth	(d) Simulation H	Evolution						
3.	The lowest level cel	lowest level cells are called as							
	(a) Composite cell	(b) Sub cell	(c) Leaf cell	(d) Parent cell					
4.	The two level circuit	its are							
	(a) AND-AND	(b) OR-OR	(c) NAND-NAND	(d) AND-NOT					
5.	Which algorithm is used for retiming minimization								
	(a) Bellman-ford Al	lgorithm	(b) Quine McCluskey Algorithm						
	(c) CAD Automatic	on Algorithm	(d) Henry Ford Algorithm						
	PART - B (5 x $3 = 15$ Marks)								

- 6. Explain the three design domains in Y chart.
- 7. Illustrate the sequence of problem formulation with suitable example.

- 8. What are the types of local routing problems?
- 9. Write short notes on Quine McCluskey algorithm.
- 10. List the components used for high level synthesis system.

PART - C (
$$5 \times 16 = 80 \text{ Marks}$$
)

11. (a) Discuss the terminology in algorithmic graph theory and explain the graph algorithm with suitable example. (16)

Or

- (b) Explain the method to find the optimal solution of a combinational optimization. (16)
- 12. (a) Explain the sequences of problem formulation with suitable examples. (16)

Or

- (b) Explain the two categories of placement algorithms. (16)
- 13. (a) Explain the shape function for a single and two inset cells and translate the sizing algorithm for slicing floor plan. (16)

Or

- (b) Discuss the global routing algorithm in detail. (16)
- 14. (a) Discuss the gate level modeling and important issues in gate level simulation. (16)

Or

- (b) Explain the Principles and manipulation of reduced ordered binary decision diagram. (16)
- 15. (a) Explain the conditional data flow and iterative data flow with suitable example. (16)

Or

(b) Briefly discuss the force directed and list scheduling algorithm with its sequence. (16)