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Question Paper Code: 27292

5 Year M.Sc. DEGREE EXAMINATION, MAY/JUNE 2016

First Semester

Computer Technology

ECT 011/ESE 012/EIT 021 - DIGITAL PRINCIPLES

(Common to: 5 year M.Sc. Information Technology and 5 Year M.Sc. Software Engineering)

(Regulations 2010)

Time: Three Hours

Maximum: 100 Marks

Answer ALL questions. $PART - A (10 \times 2 = 20 Marks)$

- 1. What is a digital system?
- 2. What is the decimal number that can be represented with 10 binary digits?
- 3. Differentiate between sequential and combinational logic circuits.
- 4. Define encoder.
- 5. What is a state table?
- 6. What is data lockout flip-flop?
- 7. What is the function of registers?
- 8. Define ring counter.
- 9. Distinguish between synchronous and asynchronous sequential logic circuits.
- 10. What are hazards in asynchronous sequential logic circuits?

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$PART - B (5 \times 16 = 80 Marks)$

- 11. (a) (i) Convert the following:
 - (1) $(F2EC)_{16} = ()_2$
 - (2) $(637)_8 = ()_{10}$.
 - (ii) Explain about laws of Boolean algebra.

OR

- (b) (i) Explain in detail about number conversions with example.
 - (ii) Design a logic circuit to convert the BCD code to Excess 3 code.
- 12. (a) Simplify the following Boolean function F, together with the don't Care conditions d, and then express the simplified function in sum of Minterms. $F(A, B, C, D) = \sum (1, 3, 5, 7, 9, 15), d(A, B, C, D) = \sum (4, 6, 12, 13).$
 - (ii) Simplify the given Boolean function using Map method F(w, x, y, z) = $\sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. (8)

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(b) Simplify the following functions, and implement them with two level NOR gate circuits.

(i)
$$F = wx' + y'z' + w'yz'$$
 (8)

- (ii) $F(w, x, y, z) = \sum (5, 6, 9, 10).$ (8)
- 13. (a) Discuss how synchronous sequential logic circuits are analysed highlighting the role of state table, state diagram and state equations in the analysis?

OR

- (b) Discuss the various types of flip flops in detail.
- 14. (a) Explain the function of 4-bit shift registers.

OR

- (b) Discuss in detail about the function of Synchronous Counters.
- Design an asynchronous circuit that has two input lines X and Y and one output line Z. If X = Y, then Z is to change so that it is the same as X and Y. Otherwise, Z does not change. In other words Z changes if it is different from all of its inputs. It does not change if it agrees with at least one of its inputs.

OR

- (b) Each of the following specifications describes a fundamental mode sequential circuit with two inputs x_1 , and x_2 and one output z. Derive a primitive and a reduced flow table for each circuit.
 - (i) When $x_2 = 1$, the value of the output z is equal to the value of x_1 ; when $x_2 = 0$, the output remains fixed at its last value prior to x_2 becoming zero.
 - (ii) The output z is equal to 0 whenever $x_1 = 0$. The first change in input x_2 , occurring while $x_1 = 1$, causes z to become 1 thereafter z remains 1, until x_1 returns to 0.

(8)