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Question Paper Code : 41918

M.E. DEGREE EXAMINATION, APRIL/MAY 2015.

Elective

VLSI Design

VL 9261/AP 954/UAP 9167/10244 VLE 11 — ASIC DESIGN

(Common to M.E. Electronics and Communication Engineering/M.E. Computer and Communication Engineering/M.E.Applied Electronics)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the ASIC design flow diagram.

2. What are the various CMOS design rules?

3. What are the two types of programmable ASICs?

4. Compare Anti fuse, SRAM, EPROM, EEPROM technologies with respect to erasing mechanism.

5. List few files created in the synthesis process of ACTEL device.

6. Mention the features of EDIF.

7. What are the data formats supported in Verilog?

8. List out types of simulation and state its application.

9. Differentiate various routing methods involved in ASIC design.

10. What do you meant by DRC and why it is needed in ASIC Design?

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail about the types of ASICs. (16)

Or

(b) Explain in detail about the CMOS transistors with its derivation. (16)

12. (a) (i) Write short notes on EPROM and EEPROM technologies used in Xilinx EPLD and Altera Max 5000 EPLD. (8)

(ii) Consider the junction F = A.B + B'.C + D. Use Shannon's expansion theorem to expand F with respect to F = B .F1 + B'. F2. (8)

Or

(b) (i) Write short notes on Meta stability. (8)

(ii) Draw and explain the block diagram of a Xilinx 4000 series IO Block. (8)

13. (a) (i) Discuss in detail about low level design languages. (8)

(ii) Write short notes on EDIF. (8)

Or

(b) (i) Draw and explain the block diagram of an Altera Max Interconnect scheme. (8)

(ii) Discuss in detail about PLA tools. (8)

14. (a) (i) Write the VHDL code for a 8 bit ripple — carry adder using full adder as a component. (8)

(ii) Explain in detail about automatic test pattern recognition. (8)

Or

(b) (i) Write a note on package and libraries of VHDL. (8)

(ii) Explain how Verilog is used to define delays with a suitable example. (8)

15. (a) (i) Explain the procedure for measurement of delay in floor planning.(8)

(ii) Explain how global routing is established between and inside blocks with suitable diagram. (8)

Or

(b) (i) Discuss the different methods of partitioning with suitable diagrams. (8)

(ii) Explain the steps involved in left edge algorithm for a two layer channel routing. (8)