12/5/15/FN
LIB/ANNA

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71686

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Fourth Semester

Instrumentation and Control Engineering

IC 2251/IC 43/EC 1263 A/10133 IC 403/080260004 — DIGITAL PRINCIPLES AND DESIGN

(Regulation 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is a code converter? List some of the code converter.
2. What is the difference between decode and demultiplexer?
3. What do you meant by race around condition?
4. What is the difference between a ring counter and a Johnson counter?
5. What is mask-programmable and field programmable logic array?
6. What is FPGA and CPLD?
7. How does open collector output differ from totem-pole outputs?
8. List the advantages of I^2L family.
9. List the characteristics of CMOS family.
10. Why does the MOS family mostly use NMOS devices?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Design and implement a 4-bit gray-to-binary converter. (10)

(ii) Realize 1 of 16 multiplexer and explain its function. (6)

Or

(b) (i) Minimize the following function using Quine Mc Clusky method.

(A, B, C, D) = Σm (3, 4, 5, 7, 9, 13, 14, 15). (8)

(ii) Design a full subtractor circuit. (8)

12. (a) (i) Show D flip flop implementation from a S-R flip flop and explain. (6)

(ii) Design a synchronous counter to count the following random sequence using J-K flip flop: 0, 1, 3. 7, 6, 5. (10)

Or

(b) (i) Explain the operation of 4-bit synchronous counter using J-K flip flop. (8)

(ii) Explain the following state assignments in connection with asynchronous sequential machine: (1) Shared row state assignment and (2) One hot state assignment. (4 + 4)

13. (a) (i) Draw and explain the internal construction of PLA having three inputs, three product terms and two outputs. (8)

(ii) Realize the following logic functions using ROM: (8)

$Y_1(A,B,C) = \Sigma m(0,2,4,7)$

$Y_2(A,B,C) = \Sigma m(1, 3, 5, 7)$.

Or

(b) (i) Design a sequence detector to detect a sequence 1101 using a suitable PLA. Give state diagram and state table. (10)

(ii) Draw and explain the block diagram of PLA. (6)

14. (a) (i) Draw and explain the operation of I^2L NAND and NOR gates. (10)

(ii) Explain the interfacing of ECL gates with CMOS and TTL gates. (6)

Or

(b) (i) Draw the circuit diagram of a ECL NOR/OR gate and explain the operation. (9)

(ii) Draw the circuit of NAND gate using CMOS and explain. (7)

15. (a) (i) Derive a CMOS complex gate for the logic function F=AB+AC+BC. (10)

(ii) Explain why are MOS ICs especially sensitive to static charge? (6)

Or

(b) (i) Explain the important characteristics of NMOS logic. (6)

(ii) Draw and explain the basic NMOS NAND and NOR gates. (10)
