Reg. No. | | | | | | | | | | | | |

Question Paper Code : 51529

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Fourth Semester

Electronics and Instrumentation Engineering

EI 2253/EI 43/080300014/10133 EE 406 – DIGITAL LOGIC CIRCUITS

(Regulations 2008/2010)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Simplify $A + AB + BC + AC$.
2. State Involution theorem.
3. Realise the logic expression $Y = \overline{AB} + A + (\overline{B + C})$ using NAND gates only.
4. What is the function of a multiplexers select inputs ?
5. How many flip-flops are required to build a binary counter that counts from 0 to 128 ?
6. Why is state reduction necessar ?.
7. What is an asynchronous sequential circuit ?
8. Give the significance of state assignment.
9. What are the uses of buffer ?
10. A certain gate draws 1.8 mA when its output is high and 3.2 mA when its output is low. What is the average power dissipation if vcc is 5v and it is operated on a 50% duty cycle.

PART – B (5 × 16 = 80 Marks)

11. (a) (i) Convert 11ABCF. 16_{16} into octal, decimal and binary number systems. **(6)**

(ii) Convert all 4-bit binary numbers into its gray equivalent. **(10)**

OR

(b) Simplify the function f(A,B, C, D) = AB'C + ABCD + A'B'C + D' using

(i) Karnaugh map **(8)**

(ii) Quine McCluskey method **(8)**

12. (a) (i) Draw the logic diagram of IC 74138 and explain the operation with truth table. **(10)**

(ii) Design a full-adder circuit using only NOR gates. **(6)**

OR

(b) (i) List the applications of magnitude comparator and multiplexer. **(6)**

(ii) Design a code converter that converts a BCD into excess 3 code. **(10)**

13. (a) Design a sequential circuit with four JK flip-flops ABCD. The next states of B, C, D are equal to the present states of A, B, C. The next state of A is equal to the X-OR of the present states of C and D. **(16)**

OR

(b) (i) Design a 4-bit bidirectional shift register. **(8)**

(ii) Design a synchronous counter using JK FF to count the following sequence 7,4, 3,1, 5, 0, 7..... **(8)**

14. (a) Design a T flip-flop from logic gates.

OR

(b) (i) An asynchronous sequential circuit is described by the following excitation and output function :

$$Y = x_1x_2 + (x_1 + x_2)y$$

$$Z = y$$

(1) Draw the logic diagram of the circuit.

(2) Derive the transition table and output map.

(3) Describe the behaviour of the circuit. **(10)**

(ii) Write notes on shared row state assignment and one hot state assignment. **(6)**

15. (a) (i) Compare PROM, PLA and PAL. **(8)**

(ii) Design a switching circuit that converts a 4 bit binary code into a 4 bit gray code using ROM array. **(8)**

OR

(b) (i) Explain the operation of ECL NOR/OR gate with neat sketch. **(10)**

(ii) Write the characteristics of ECL family. **(6)**