Reg. No. | | | | | | | | | | | | |

Question Paper Code : 51540

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Seventh Semester

Electrical and Electronics Engineering

EI 2403/EI 73 – VLSI DESIGN

(Common to Instrumentation and Control Engineering/Electronics and Instrumentation Engineering)

(Regulations 2008)

(Also common to 10144 EC 605 – VLSI Design for B.E. (Part-Time) Seventh Semester EEE – Regulations 2010)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Define drain punchthrough.
2. Mention the problems caused if the gate oxide layer of MOS transistors is very thin.
3. What are the drawbacks of NMOS inverters compared with CMOS inverters ?
4. Write the pull up/pull down ratio required when an inverter is driven through pass transistors.
5. Name any one fast adder and fast multiplier.
6. Implement Y = (A + B) (C + D) using NOR-NOR logic.
7. What are the different ways to program the PAL ?
8. Define FSM.
9. Write the behavioral VHDL code for a SR latch.
10. Write a structural VHDL code for a 4:1 MUX.

PART – B (5 × 16 = 80 Marks)

11. (a) Draw and explain the steps involved in the fabrication of NMOS transistor. Discuss the additional steps required for CMOS fabrication with suitable diagrams. **(16)**

OR

(b) (i) Write the equations for the NMOS transistor current in different regions of operation and explain. Discuss the effects of channel length modulation on the current equations. **(8)**

(ii) Draw and explain the small signal model for NMOS transistors. **(8)**

12. (a) (i) Draw the stick diagram and layout of a NMOS inverter. **(8)**

(ii) Explain the operation of an inverting and a noninverting NMOS superbuffer. **(8)**

OR

(b) (i) Draw and explain the operation of a BiCMOS inverter and a two input BiCMOS NOR gate. **(4+6)**

(ii) Give a brief note on the theory and design of pass transistor logic. **(6)**

13. (a) (i) Draw the circuit of 2 input NAND gate using static CMOS design and explain. **(8)**

(ii) Explain in detail about the working principle of 4 × 4 barrel shifter. **(8)**

OR

(b) Explain the different CMOS implementation of 4 to 1 multiplexer. **(16)**

14. (a) (i) Compare PLA and PAL devices. **(6)**

(ii) Discuss the finite state machine implementation of BCD to Excess 3 code converter in PLA. **(10)**

OR

(b) Describe the architecture of FPGA with Configurable Logic Block and Programmable interconnect technology.

15. (a) Write the behavioral and structural VHDL code and test bench program for a JK Flip-flop.

OR

(b) Write a behavioral VHDL code and test bench program for a 4-bit synchronous gray code counter.