Reg. No. | | | | | | | | | | | | |

**Question Paper Code : 51374**

**B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016**

**Seventh Semester**

**Electrical and Electronics Engineering**

**CS 2071/CS 608/10133 EEE 24 – COMPUTER ARCHITECTURE**

**(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)**

**(Regulations 2008/2010)**

**(Common to PTCS 2071 – computer Architecture for B.E. (Part-Time) Sixth Semester – EEE – Regulations 2009)**

**Time : Three Hours** **Maximum : 100 Marks**

**Answer ALL questions.**

**PART – A (10 × 2 = 20 Marks)**

1. What are the major components of Computer Architecture ?
2. Mention the advantage of using assembly language.
3. What is the multiply rule for floating point numbers ?
4. Draw the diagram of a basic cell that can be used in each bit stage of an adder.
5. Give any two reasons for pipeline stalls.
6. What is Microprogram sequencer ?
7. Differentiate DRAM Vs SRAM.
8. List various cache memory design parameters.
9. Define nested interrupts with example.
10. Define multithreaded processors.

## PART – B (5 × 16 = 80 Marks)

11. (a) (i) Explain the von Neumann architecture of computing systems. **(8)**

(ii) Describe addressing modes of instructions with suitable examples. **(8)**

**OR**

(b) (i) List and explain with suitable examples the types of instructions of general processor instruction Set. **(8)**

(ii) Compare and contrast between the combinational and sequential logics. **(8)**

12. (a) (i) Starting from the truth table explain how to construct a full adder. **(8)**

(ii) What is a ripple carry adder ? Mention its disadvantage and explain how is it resolved. **(8)**

**OR**

(b) Design a floating point adder unit and explain the process of addition with a flow chart. **(16)**

13. (a) (i) Describe the micro programmed control unit with neat sketch. **(8)**

(ii) Explain data hazard with example. **(8)**

**OR**

(b) (i) What is branch prediction. Explain static and dynamic branch prediction approaches. **(10)**

(ii) Explain superscalar operation in detail. **(6)**

14. (a) (i) Explain about SRAM and DRAM. **(8)**

(ii) Discuss about Virtual memory. **(8)**

**OR**

(b) (i) Explain about cache memory. **(8)**

(ii) Discuss about RAID. **(8)**

15. (a) (i) Explain the Accessing mechanism of I/O Devices. **(8)**

(ii) Explain the Enabling and Disabling Interrupts mechanism handled by a processor. **(8)**

**OR**

(b) Define DMA. Explain the process of DMA with necessary buses and interfaces. **(16)**