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Question Paper Code : 51505

B.E/B. Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Fourth Semester

Electrical and Electronics Engineering

EE 2255/EE 46/EC 1261 A/080280029/10133 EE 406 A – DIGITAL LOGIC CIRCUITS

(Regulations 2008/2010)

(Common to PTEE 2255/10133 EE 406 – Digital Logic Circuits for B.E. (Part-Time) Third Semester – EEE – Regulations 2009/2010)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Simplify the expression using Boolean Algebra ((AB' + ABC)' + A(B + AB'))'.
2. Realize the OR functions using 2.1 MUX.
3. Draw the logic diagram of master slave D- Flip Flop using NAND gates.
4. Reduce the number of states in the following table and tabulate the reduced state table.

Present State	Next State		Output	
	X = 0	X = 1	X = 0	X = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

5. Investigate the following transition table and determine any two race conditions. Explain whether they are critical or non critical.

y_1y_2 \ x_1x_2	00	01	11	10
00	10	(00)	11	10
01	(01)	00	10	10
11	01	00	(11)	(11)
10	11	00	(10)	(10)

6. An asynchronous sequential circuit is described by the following excitation and output functions, obtain a 2-state flow table.

$$Y = x_1x_2' + (x_1 + x_2')\,y$$

$$z = y$$

7. What is mask programmable and field programmable logic array ?

8. Why CMOS is preferred over other digital logic families ?

9. Write a test bench for Half adder using VHDL.

10. Consider a = 1010 and b = 1100 and Y = a + b (a.b). Compute the value of Y in VHDL.

PART – B (5 × 16 = 80 Marks)

11. (A) (i) Obtain the Reduced Boolean Expression for the following using Quine McKlusky method and find the essential and non-essential prime implicants. **(8)**

$F(A, B, C, D) = \Sigma (0, 1, 4, 5, 9, 10, 12, 14, 15) + \Sigma d (2, 8, 13)$

(ii) Define propagation delay. Construct a four bit adder circuit which first determines the carry for all the stages and produces the sum. Write the Boolean expressions for all the carry generated. **(8)**

OR

(B) (i) Construct BCD to Seven Segment Decoder using Karnaugh Map and compare the Complexity of the circuit when it is Implemented with 4X16 Decoder. **(8)**

(ii) Using a 4-to-16 line decoder constructed from NAND gates and having an enable input E', design an excess -3 to 8421 code converter. **(8)**

12. (A) (i) A sequential circuit has two JK flip-flops, A and B; two inputs, x and y; and one output z. The flip-flop input functions and the circuit output functions are as follows : **(8)**

$J_A = Bx + B'y'$ $K_A = B'xy'$

$J_B = A'x$ $K_B = A + xy'$

$z = Axy + Bx'y'$

(a) Draw the logic diagram of the circuit.

(b) Tabulate the state table.

(c) Derive the next state equation for A and B.

(ii) Design a modulo-5 synchronous counter using JK flip-flop. **(8)**

OR

(B) (i) Design a counter with T-Flip Flops that goes through the following binary repeated sequence : 0, 1, 3, 7, 6, 4. show that when 2 and 5 are taken to be don't care conditions, the counter may not operate property. **(8)**

(ii) A sequential, circuit, has two JK flip flops A and B and one input x. The circuit is described by the following flip-flop input equation. **(8)**

$J_A = X$ $K_A = B'$

$J_B = X$ $K_B = A$

(a) Derive the state equations A(t+l) and B(t+l) by substituting the input equations for the J and, K variable.

(b) Draw the state diagram of the circuit.

13. (A) (i) Construct two input TTL NAND gate with three states output and explain its operation. Also discuss its merits and demerits. **(8)**

(ii) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the complement of the input number. **(8)**

OR

(B) (i) A combinational circuit is defined by the functions : **(8)**

$F_1(A,B,C) = \Sigma (3, 5, 6, 7)$

$F_2(A,B,C) = \Sigma (0, 2, 4, 7)$

Implement the circuit with a PLA having three inputs, four product terms, and two outputs.

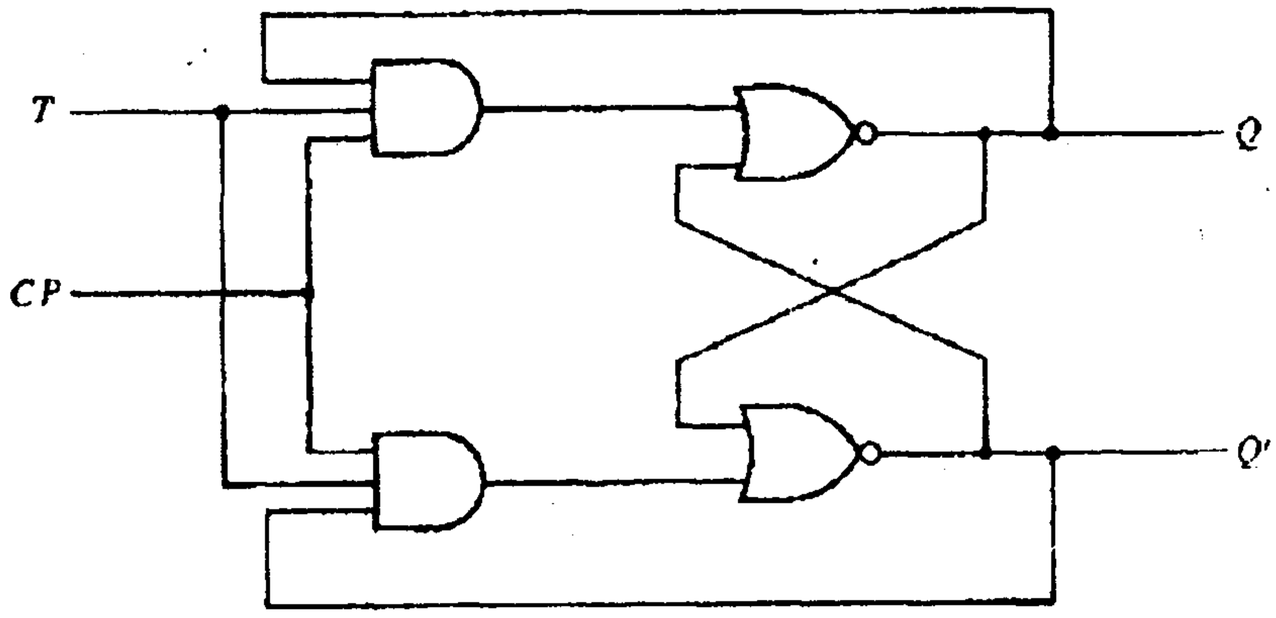
(ii) Derive the PLA programming table for the combinational circuit that squares a 3-bit number. Minimize the number of Product terms. **(8)**

14. (A) (i) The Boolean functions for the inputs of an SR latch are as follows, obtain the circuit diagram using a minimum number of NAND gates. **(8)**

$S = x'_1 x'_2 x_3 + x_1 x_2 x_3$

$R = x_1 x'_2 + x_2 x'_3$

(ii) Analyze the T flip-flop shown in the circuit below. Formulate the transition table and show that the circuit is unstable when both T and CP are equal to 1. **(8)**



OR

(B) (i) Derive a primitive flow table for a circuit with two inputs, x_1 and x_2, and two outputs, z_1 and z_2, that satisfy the following conditions : **(8)**

(a) When $x_1x_2 = 00$, the output is $z_1z_2 = 00$.

(b) When $x_1 = 1$ and x_2 changes from 0 to 1, the output is $z_1z_2 = 01$.

(c) when $x_2 = 1$ and x_1 changes from 0 to 1, the output is $z_1z_2 = 10$

(d) Otherwise, the output does not change.

(ii) Explain the difference between asynchronous and synchronous sequential circuits and define the following : **(8)**

(a) Fundamental Mode of operation of Circuits.

(b) Transition Table, Excitation Table, Primitive Flow Table.

(c) Mealy and Moore Machines.

15. (A) (i) Write a VHDL Module that describes a 16-bit serial in serial out shift register with input SI (serial Input), EN (Enable) and CK (Clock shifts on rising edge) and a serial output (SO). **(10)**

(ii) Write a data flow VHDL for Full subtractor using logic equations. **(6)**

OR

(B) (i) Write the VHDL program in mixed style to design a synchronous counter to count even number. Write the test bench program to test the circuit operation. **(10)**

(ii) List out and explain different operator used in VHDL programming. **(6)**