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Question Paper Code : 51444

B.E. /B. Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 – DIGITAL ELECTRONICS

(Regulations 2008/2010)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester – Electronics and Communication Engineering Regulations 2009)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Simplify $f(x, y) = x'y + xy + xy'$.

2. Implement EXOR function using NAND gates only.

3. Design a Half Subtractor.

4. What is a parity bit ? Give the odd parity and even parity bits for the data 10.

5. State the difference between edge triggering and level triggering.

6. Give one application of a ring counter.

7. What is an EEPROM ?

8. State the difference between PAL and PLA.

9. What is a pulse mode asynchronous sequential circuit ?

10. What are the parts of a module in verilog ?

PART – B (5 × 16 = 80 Marks)

11. (a) (i) State and prove consensus theorem. **(6)**

(ii) Minimize the following function using Karnaugh Map : **(10)**

$f(A, B, C, D, E) = \Sigma m(0, 2, 5, 6, 8, 11, 12, 13, 16, 18, 20, 28, 30, 31)$

OR

(b) (i) State and prove De Morgan's theorem. **(6)**

(ii) Minimize the following function using Quine Mc Cluskey Method. **(10)**

$f(A, B, C, D, E) = \Sigma m\ (0, 1, 3, 5, 6, 7, 9, 10, 12, 13, 17, 19, 20, 25, 26, 29, 30)$

12. (a) (i) Design and explain the operation of a Carry Look-ahead adder. **(8)**

(ii) Design a 3 × 3 Binary (Array) Multiplier. **(8)**

OR

(b) (i) Explain the operation of a 8 ×1 Multiplexer and Implement the following function using a suitable Multiplexer **(8)**

$F(A, B, C, D) = \Sigma m\ (0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)$

(ii) Design a magnitude comparator to compare two 3-bit numbers : **8**

$A = A_2A_1A_0$ and $B = B_2B_1B_0$

13. (a) With logic diagram, characteristic table and characteristic equation explain the operation of a

(i) D Flip-Flop **(5)**

(ii) T Flip-Flop **(5)**

(iii) JK Flip-Flop **(6)**

OR

(b) (i) Design a 3-bit synchronous up/down Modulo 5 counter. **(8)**

(ii) With neat sketch, explain the operation of a 3-bit universal shift register. **(8)**

14. (a) (i) With timing waveforms, explain the memory read/write operation. **(8)**

(ii) What is memory expansion ? Explain. **(8)**

OR

(b) (i) Design a 3×8 decoder and Implement it using a suitable PLA. **(8)**

(ii) Design a 3-bit majority logic circuit and Implement it using a suitable PAL. **(8)**

15. (a) Design a sequence detector to detect the sequence 1010. Use the Algorithmic State Machine (ASM) Chart for the design. **(16)**

OR

(b) (i) What is an incompletely specified state machine ? Explain. **(8)**

(ii) Write the verilog code to realize a Full Adder using structural Modelling (Module instantiation). **(8)**
