Reg. No. | | | | | | | | | | | | |

Question Paper Code : 51464

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Eighth/Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64/10144 EC 704 – VLSI DESIGN

(Common to Biomedical Engineering)

(Regulations 2008/2010)

(Common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulations 2009)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Determine the drain current of short channel NMOS transistor for the following measurements V_{DS} = 1.5 V, V_{GS} = 2 V, V_{BS} = 0 V, V_{TO} = 0.43 V. Assume V_{DSAT} = 0.6 V, K_n = 110 uA/V^2, λ = 0.1 V^{-1}, γ = 0.4 and W/L = 0.4/0.25.
2. Define any two Layout design rules.
3. Give the effect of supply voltage and temperature variations on the CMOS system performance.
4. What are the factors that cause static power dissipation in CMOS circuits ?
5. Implement a 2:1 Mux using pass transistor.
6. Design a one transistor DRAM cell.
7. What is the need for testing ?
8. What is the principle behind logic verification ?
9. Give the comparison between structural and switch level modeling.
10. What are gate primitives ?

PART – B (5 × 16 = 80 Marks)

11. (a) Explain the DC transfer characteristics of CMOS inverter. **(16)**

OR

(b) (i) Explain in detail of C-V Characteristics of MOSFET. **(8)**

(ii) Explain any one process enhancement method and one manufacturing issue in detail. **(8)**

12. (a) (i) Explain the different factors that affects the reliability of CMOS chips. **(8)**

(ii) Discuss the principle of constant field and lateral scaling. Write the effects of the above scaling methods on the device characteristics. **(8)**

OR

(b) (i) Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors. **(8)**

(ii) Give a brief note on logical effort and transistors sizing. **(8)**

13. (a) (i) Implement Y = (A + B)(C + D) using the standard CMOS logic. **(8)**

(ii) Implement NAND gate using pseudo-nMOS logic. **(8)**

OR

(b) (i) Implement D-flip-flop using transmission gate. **(8)**

(ii) Implement 2-bit non-inverting dynamic shift register using pass transistor logic. **(8)**

14. (a) Explain the Boundary Scan testing.

OR

(b) Explain the logic verification in detail.

15. (a) Design and develop the HDL project to realize the function of a priority encoder using structural model. **(16)**

OR

(b) (i) Write a data-flow model verilog HDL program for the two input comparator circuit. **(8)**

(ii) Write a behavioural level verilog HDL program for the 1 × 8 multiplexer circuit. **(8)**
