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Question Paper Code : 51393

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Sixth Semester

Computer Science and Engineering

CS 2354/CS 64/10144 CS 604 – ADVANCED COMPUTER ARCHITECTURE

(Regulations 2008/2010)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. What is Instruction Level Parallelism ?

2. How many branch-selected entries are in a (2, 2) predictor that has a total of 8k bits in the prediction buffer ?

3. List any two limitations of Instruction Level Parallelism.

4. What are the parts of 10-stage pipelining in itanium processor ?

5. What is multiprocessor cache coherence ?

6. Define sequential consistency.

7. How is a block found in the cache ?

8. Define average memory access time.

9. What is simultaneous multithreading ?

10. List any four important features of IMB cell processor.

PART – B (5 × 16 = 80 Marks)

11. (a) Explain Dynamic scheduling using Tomasulo's approach.

OR

(b) Discuss in detail about the hardware based speculation.

12. (a) Discuss the hardware support for exposing more parallelism at compile time.

OR

(b) Explain the Intel IA-64 instruction set architecture.

13. (a) Discuss the performance of distributed shared-memory multiprocessors.

OR

(b) Explain in detail about the Multithreading in ILP.

14. (a) Explain the techniques in reducing cache miss penalty.

OR

(b) Explain in detail about RAID levels.

15. (a) Explain the architecture of SUN CMP processor.

OR

(b) Discuss the design issues in SMT & CMP architectures.
