Reg. No. | | | | | | | | | | | | |

Question Paper Code : 51381

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Fourth Semester

Computer Science and Engineering

CS 2253/CS 43/CS 1252 A/080250011/10144 CS 404 – COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulations 2008/2010)

(Also Common to PTCS 2253 – Computer Organization and Architecture for B.E. (Part-Time) Third Semester – CSE – Regulations 2009)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. State the basic performance equation.

2. What do you mean by an interrupt ?

3. Compare hardwired and micro programmed controls.

4. What is nano programming ?

5. What is a hazard ?

6. Define exception.

7. An address space is specified by 24 bits and the corresponding memory space by 16 bits :

   How many words are there in the virtual memory and in the main memory ?

8. What is meant by an interleaved memory ?

9. Why are interrupt masks provided in any processor ?

10. What is the necessity of an interface ?

PART – B (5 × 16 = 80 Marks)

11. (a) (i) Explain the different types of instructions with examples. Compare their relative merits and demerits. **(8)**

(ii) Explain with an example how to multiply two unsigned binary numbers. **(8)**

OR

(b) Explain the design of ALU in detail. **(16)**

12. (a) (i) Explain in detail the control sequence for an unbranch instruction, unconditional and conditional branch instruction. **(12)**

(ii) Give the control sequence for the instruction Add R4, R5, R6. **(4)**

OR

(b) Discuss about the hardwired control in detail. **(16)**

13. (a) (i) Explain the performance of pipelining. **(8)**

(ii) Explain in detail about the limitations of ILP. **(8)**

OR

(b) Explain in detail the various pipeline hazards and methods to overcome them. **(16)**

14. (a) (i) Explain the need for memory hierarchy technology, with a four-level memory. **(6)**

(ii) Explain the various mapping techniques associated with cache memories. **(10)**

OR

(b) (i) Explain a method of translating virtual address to physical address. **(6)**

(ii) What for replacement algorithms are used ? Explain the important ones. **(10)**

15. (a) What is an interrupt ? Explain the different types of interrupts and the different ways of handling interrupts. **(16)**

OR

(b) (i) Write and explain the working of Peripheral Components Interconnect (PCI) Bus. **(8)**

(ii) Discuss DMA controller with block diagram. **(8)**