Reg. No. : | | | | | | | | | | |

Question Paper Code: 31036

B.E. / B.Tech. DEGREE EXAMINATION, OCTOBER 2014.

Third Semester

Electrical and Electronics Engineering

01UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Draw the CMOS Inverter circuit.
2. Convert $(0.95)_{10}$ to its binary equivalent.
3. Simplify $y = \Sigma m(1,3,5,7)$.
4. Draw the logic diagram of half subtractor.
5. Differentiate level triggering and edge triggering?
6. How many flip flops are required to implement the Mod-6 counter and write the truth table for same?
7. What is meant by stuck-at-0 and stuck-at-1 fault?
8. What are the advantages of providing input buffer and output buffer in digital logic circuits?
9. Give any two features of VHDL.
10. What do you mean by system Library and user Library?

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Determine the single error correcting code for the information code 10111 for odd parity. (8)

(ii) Write notes on Reflective code, Sequential code, Excess 3 code and Hollerith code with example. (8)

Or

(b) (i) Explain the circuit operation of 3 input TTL NAND logic with neat sketch. (8)

(ii) Discuss the characteristics of MOS families. (8)

12. (a) (i) Design 1:8 demultiplexer using 1:4 demultiplexers. (6)

(ii) Implement the following Boolean function with suitable multiplexer. $(A,B,C,D)=\Sigma m\ (0,2,6,10,11,12,13) + d(3,8,14)$. (10)

Or

(b) (i) Simplify $y = \pi(0,1,4,5,6,8,9,12,13,14)$ using K - map method. (10)

(ii) Write notes on incompletely specified function with suitable examples. (6)

13. (a) (i) Realize the JK flip - flop using D flip - flop. (10)

(ii) Discuss the 2 bit synchronous counter with timing diagram. (6)

Or

(b) Explain the working of different types of 4 bit shift register. (16)

14. (a) Design a pulse mode circuit having two input lines X_1 and X_2 and one output line Z. The circuit should produce an output pulse to coincide with the last input pulse in the sequence $X_1X_2\ X_2$. No other input sequence should produce an output pulse. (16)

Or

(b) (i) Realize the given function using 3X4X2 PLA.

$f_1 = \Sigma m\ (0,1,3,4)$
$f_2=\Sigma m(1,2,3,4,5)$ (8)

(ii) Compare PROM, PLA and PAL. (8)

15. (a) Write notes on

(i) Basic components of RTL design
(ii) Arithmetic Micro operations
(iii) Logic Micro operations
(iv) Conditional control statements. (16)

Or

(b) Explain the working of synchronous MOD 6 counter and write VHDL code for synchronous MOD 6 counter. (16)

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