Reg. No. : | | | | | | | | | | |

Question Paper Code: 31042

B.E. / B.Tech. DEGREE EXAMINATION, OCTOBER 2014.

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Convert the decimal number 34.435 to binary.
2. State De Morgan's theorems. Simplify the expression Y(A,B,C,D) = [A(B+C')'D]' using it.
3. Draw the logic diagram of a half subtractor with inputs X, Y and outputs D, M using gates.
4. How does a carry look ahead adder speed up addition process?
5. Draw the logic symbol and truth table of T flip flop.
6. The content of a 4 bit register is initially 1101. The register is shifted six times to the right with serial input of 101101. What is the content of the register with each shift?
7. Compare the features of PROM, PLA and PAL.
8. Differentiate static and dynamic RAM.
9. What is the difference between synchronous and asynchronous sequential circuits?
10. Distinguish between static and dynamic hazards.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) What are maxterms and minterms? Express Y(A,B,C) = AB + A'C as a sum of minterms. (6)

(ii) Using K map find the minimized expression for the following function $F(w,x,y,z) = \Sigma(0,2,4,5,6,7,8,10,13,15)$. (5)

(iii) Using K map find the minimized expression for the following function

$F(A,B,C,D) = \Pi(0,2,3,6,7,8,10,12,13)$. (5)

Or

(b) (i) Demonstrate that a 2 input NAND gate is a universal logic element. (6)

(ii) Find the set of essential prime implicants and minimize the function $F(A,B,C,D,E) = \Sigma m(1,3,4,6,7)$ using Quine Mcclusky method and clearly explain the various steps. (10)

12. (a) Design a 4 bit magnitude comparator using logic gates. (16)

Or

(b) (i) Implement the following Boolean function with Multiplexer
$F(A,B,C,D) = \Sigma(0,1,3,4,8,9,15)$ (8)

(ii) Explain 4 bit binary parallel adder with a neat diagram. (8)

13. (a) (i) With a neat sketch explain the function of 4 bit synchronous up/down counter. (10)

(ii) Realize a SR flip flop using NAND gates and give its truth table. (6)

Or

(b) Design 3 bit binary counter using T flip flop. Give the state table, state diagram and logic diagram. (16)

14. (a) (i) Implement the following Boolean function using PLA
$F1(a,b,c) = \Sigma(0,1,2,4)$, $F2(a,b,c) = \Sigma(0,5,6,7)$, $F3(a,b,c) = (0,3,5,7)$ (10)

(ii) Write short notes on FPGA. (6)

Or

(b) Draw the logic construction of 4*4 RAM memory cell and explain how data can be read from it. Also show the timing diagram of a read cycle for a static RAM. (16)

15. (a) Explain races and hazards that occur in asynchronous sequential circuits and the design of a hazard free circuit with an example. (16)

Or

(b) Design a asynchronous sequential circuit for negative edge triggered T flip flop. (16)
