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Question Paper Code: 49271

M.E. DEGREE EXAMINATION, DECEMBER 2014.

First Semester

VLSI Design

14PVL507 – ASIC DESIGN TECHNIQUES

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (5 x 1 = 5 Marks)

1. Storage loop that hold its state as long as the power is 'ON' is called as

   (a) Dynamic latch (b) Domino latch (c) Static latch (d) both (a) & (c).

2. EPROM Technology consists of

   (a)Double gate (b) Single gate (c) Floating gate (d) Triple gate

3. How many macro cells exist in each LAB of alteramax 9000?

   (a) 8 (b) 16 (c) 24 (d) 48

4. Short circuit fault which occur in interconnect is called as

   (a) Stuck at fault (b) Bridging fault (c) Delay fault (d) Fault effect

5. Each ATM cell has

   (a) 53 byte (b) 63 byte (c) 42 byte (d) 55 byte

PART - B (5 x 3 = 15 Marks)

6. Mention the important features of programmable logic devices.
7. What is the state of metastability?
8. Give the significance of EDIF.
9. Define timing analysis.
10. Describe simulated annealing process.

PART - C (5 x 16 = 80 Marks)

11. (a) (i) Discuss about the CMOS transistor and CMOS design rules. (8)

(ii) Discuss the different types of gate array based ASIC. (8)

Or

(b) (i) Briefly explain the logical effort and also determine various delays involved in logical effort. (8)

(ii) Describe the library cell design and its architecture. (8)

12. (a) (i) Explain about Antifuse operation in detail. (8)

(ii) Explain XC4000 logic block with neat sketch. (8)

Or

(b) (i) Discuss in detail about the Altera Max DC and AC input and ouputs. (8)

(ii) Describe about the xilink I/O blocks. (8)

13. (a) (i) Describe the Xilinx LCA interconnect Architecture with neat sketch. (8)

(ii) Illustrate and explain the Altera max 7000 series architecture. (8)

Or

(b) (i) Explain in detail about the hierarchical nature of an EDIF file. (8)

(ii) Write short notes on PLD programming languages. (8)

14. (a) Explain in detail about boundary scan test in detail. (16)

Or

(b) (i) Discuss the types of fault and its simulation. (8)

(ii) Describe the automatic test pattern generation in detail. (8)

15. (a) Illustrate the partitioning steps involved in the Kernighan-lin algorithm with an example. (16)

Or

(b) (i) Explain the Eigen value placement with an example. (8)

(ii) Examine the global routing method using gate array. (8)

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