Reg. No. : | | | | | | | | | | |

Question Paper Code: 92073

M.E. DEGREE EXAMINATION, OCTOBER - 2014.

Elective

VLSI Design

01PVL519 – SYSTEM DESIGN USING FPGA

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Draw the generalized block diagram of FPGA.
2. Distinguish between PAL and PLA.
3. Differentiate between coarse grained and fine grained architectures of FPGA.
4. Draw a switching matrix used in programmable interconnects.
5. Mention the different ways of Design entry for FPGA based design.
6. Expand JTAG and give its significance.
7. Mention the advantage of Verilog HDL over other HDLs.
8. Give any two sequential statements used in Verilog HDL.
9. List the different types of fault models used in digital circuits.
10. Define formal verification.

PART - B (5 x 14 = 70 Marks)

11. (a) (i) Compare the FPGA and CPLD design flow for implementing digital circuits. (10)

(ii) Explain about the Programmable Logic Element. (4)

Or

(b) Explain the various available programming techniques for FPGA and discuss about their significance for the market requirement. (14)

12. (a) (i) Describe the principle of implementing logic expression in Xilinx XC3000 logic block with neat diagram. (10)

(ii) Illustrate the process of configuring I/O block of an FPGA. (4)

Or

(b) (i) Briefly explain the logic block of Xilinx XC5200 series with neat diagram. (7)

(ii) Explain the operation of programmable interconnect in Xilinx FPGA. (7)

13. (a) Explain the process of technology mapping in FPGA design flow. (14)

Or

(b) Describe in detail about the functional simulation and timing simulation. (14)

14. (a) Explain about the Data flow modeling and Behavioural modeling in Verilog HDL with suitable examples. (14)

Or

(b) Explain the method of designing synchronous circuits using Verilog HDL with example. (14)

15. (a) Briefly explain about Built - In Self Test with neat diagram (14)

Or

(b) Describe Reconvergent Fanout and the way to overcome with an example. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Given a logic expression $F(a, b, c, d) = \sum m(1, 3, 5, 9, 15) + d(2, 4, 12)$. Show the implementation of the expression using PAL, PLA and CPLD. (10)

Or

(b) Write a verilog HDL program for a synchronous sequential mod-4 counter. (10)