Reg. No. : | | | | | | | | | | |

Question Paper Code: 92072

M.E. DEGREE EXAMINATION, OCTOBER - 2014.

Elective

VLSI Design

01PVL508 - TESTING OF VLSI CIRCUITS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. When is a fault said to be detectable?
2. Distinguish between compiled simulation and event - driven simulation.
3. What is the need for backtracking strategy during test pattern generation?
4. Define detection quality of a test sequence.
5. State the difference between fully integrated serial scan and isolated serial scan.
6. What are the important factors that determine the complexity of deriving a test for a circuit?
7. State the techniques used for generating test pattern for pseudo exhaustive test.
8. What are the disadvantages of Random - test Socket test approach?
9. What is meant by fault dictionary?
10. Mention the need for self - checking circuits.

PART - B (5 x 14 = 70 Marks)

11. (a) (i) Explain the concept of fault equivalence and fault localization in combinational and sequential circuits with specific examples. (7)

(ii) Discuss the parallel fault detection technique. (7)

Or

(b) (i) Explain the three valued deductive simulation techniques. Discuss its limitations. (7)

(ii) Describe the steps involved in event driven simulation. (7)

12. (a) (i) How is the detection probability of faults determined? (7)

(ii) Explain the simulation based test pattern generation approach. (7)

Or

(b) Explain the method of test generation using iterative array model for sequential circuit using specific example. (14)

13. (a) (i) Explain the significance of test point in Ad Hoc design. (7)

(ii) List the various factors that determine the selection of control points and observation points. (7)

Or

(b) Explain the various generic scan based designs. (14)

14. (a) What are the techniques available for test-pattern generation for BIST architecture to perform pseudo exhaustive testing? Explain. (14)

Or

(b) Discuss the generic off - line BIST architecture. (14)

15. (a) Explain the effect - cause analysis of diagnosis by UUT reduction. (14)

Or

(b) (i) Discuss the usage of error detecting and correcting codes. (10)

(ii) What are the methods available to detect multiple - bit errors? (4)

PART - C (1 x 10 = 10 Marks)

16. (a) Let N be a combinational circuit composed of NAND gates. Assume that every primary input has only one fan - out. Show that a test set that detects all s - a - 1 faults in N detects all s - a - 0 faults as well. (10)

Or

(b) For the circuit shown

(i) Compute signal probabilities

(ii) Compute the detection probability for the fault g s - a - 0. (10)