Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 45871

5 Year M.Sc. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

First Semester

Software Engineering

XCS 115/10677 SW 105 — PROBLEM SOLVING TECHNIQUES

(Common to 5 Year M.Sc. Computer Technology and M.Sc. Information Technology)

(Regulation 2003/ 2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Add $(83)_{10}$ and $(34)_{10}$ in BCD.

2. Simplify AB + ABC + AB'.

3. Realize using NAND gates only $Y = A + A'B + AB$.

4. Differentiate a decoder and a encoder.

5. What is a Latch?

6. Give the HDL code for SR flip-flop.

7. Compare synchronous and Asynchronous counter.

8. Draw the timing diagram for a 2 bit ripple up counter.

9. What is a Hazard?

10. Define Asynchronous sequential circuit.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Reduce the following expression and implement using basic gates and then implement it using only NAND gates.

$Y = ((AB)'+(A + B)')AB'$. (4)

(ii) Draw the logic diagram of EXNOR using only NOR gates. Prove it using De-Morgan's theorem. (12)

Or

(b) (i) Simplify AB + (AC)' + A (BC)' (AB + C). (6)

(ii) Find the complement of $x(y'z) + yz$. (6)

(iii) Convert decimal 46 to gray to code. (4)

12. (a) (i) Reduce using k-map

$F = \pi\ (0, 6, 7, 8, 12, 13, 14, 15)$. (6)

(ii) Explain Binary Multiplier with a neat diagram. (10).

Or

(b) Design a carry look ahead adder.

13. (a) Design a sequence detector to detect the following sequence 1010. Draw state diagram, state table and k-map. Remove redundant states. Use JK flip-flops.

Or

(b) Design a sequential circuit with 4 Flip-Flops ABCD. The next states of B,C, D are equal to present states of A,B,C respectively. The next state of D is EXOR of the present states of C and D.

14. (a) Draw a 5 flip-flop shift counter is transition table and waveforms. Explain its operation as a decade counter.

Or

(b) (i) Design a mod5 ripple counter using a 3 bit ripple counter. (8)

(ii) Draw and explain the function of 3 bit bidirectional shift register using JK flip-flops. (8)

15. (a) An asynchronous sequential circuit is described by the excitation and ouput function. $Y = x_1 x_2' + (x_1 + x_2')\, y$ and $Z = y$.

where Y and Z are excitation and output functions respectively.

(i) Draw the logic diagram of the circuit.

(ii) Derive Transition table and output map.

(iii) Obtain the flow table.

(iv) Describe the behavior of the circuit.

Or

(b) (i) Give the hazard free realization for the following Boolean function

$f(a, b, c, d) = \Sigma m(1, 3, 4, 5, 6, 7, 9, 11, 15)$

(ii) Analyze the circuit by deriving.

(1) Flow table

(2) Transition flow diagram and

(3) Transition flow table if exists.