Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 45264

5 Year M.Sc. DEGREE EXAMINATION, JANUARY 2015.

First Semester

Computer Technology

ECT 011/EIT 021/ESE 012 — DIGITAL PRINCIPLES

(Common to 5 Year M.Sc. Information Technology/M.Sc. Software Engineering/
M.Sc. Software Systems)

(Regulation 2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Show that a positive logic AND gate is a negative logic OR gate.

2. Write the general syntax for entity declaration in VHDL.

3. Realize OR logic function using 2 : 1 Multiplexer.

4. Implement a full adder with two half adders and external gates.

5. How will you convert a JK – FF into a T – FF?

6. What is a latch?

7. Draw the state diagram of a 2 bit up counter.

8. What is the difference between serial and parallel transfer?

9. Distinguish between combinational and sequential logic circuits.

10. When do essential hazards occur?

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Convert hexadecimal 2AB5.D to decimal, octal and binary. (3)

(ii) State and prove De Morgan's theorem. (5)

(iii) Express the following function in sum of minterms and product of maxterms.

$F(w, x, y) = (xy + z)(y + xz)$. (8)

Or

(b) (i) Perform the BCD addition of 184 and 576. (4)

(ii) Given the Boolean function :

$F = xy + x'y' + y'z$.

(1) Implement it with AND, OR and NOT gates.

(2) Implement it with only OR and NOT gates.

(3) Implement it with only AND and NOT gates. (6)

(iii) Convert the following to the other canonical form :

(1) $F(x, y, z) = \pi(0, 3, 6, 7)$

(2) $F(A, B, C\,D) = \Sigma(0, 2, 6, 11, 13, 14)$. (6)

12. (a) (i) Simplify using Karnaugh map the following Boolean function :

$F = A'B'C' + B'CD' + A'BCD' + AB'C'$. (6)

(ii) Explain a 4 bit magnitude comparator. (10)

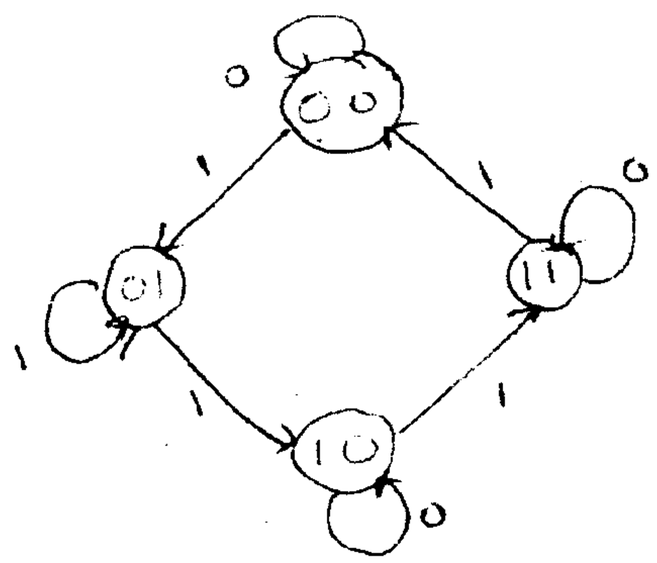
Or

(b) (i) Determine the prime-implicants of the function :

$F(w, x, y, z) = \Sigma(1, 4, 6, 7, 8, 9, 10, 11, 15)$ (12)

(ii) Implement a full subtractor with two half subtractors and an OR gate. (4)

13. (a) (i) Design a clocked sequential circuit whose state diagram is given below. Use JK flip flop.



Design a counter with the following binary sequence 0, 1, 3, 7, 6, 4 and repeat. Use T flip flop. (8)

(ii) Explain state assignment and state reduction with suitable example. (8)

Or

(b) (i) Explain the working of Master/Slave JK flip flop. Explain its operation and explain how the race around condition is eliminated. (6)

(ii) Draw and explain with timing diagram a 4-bit binary ripple up counter. (10)

14. (a) (i) How can ring counter be converted to a Johnson counter? Draw the circuit of a Johnson counter with ten timing signals.. (8)

(ii) Design a 4 bit Universal shift register and explain its operation. (8)

Or

(b) (i) Distinguish between synchronous and asynchronous sequential logic circuits. (4)

(ii) Design a synchronous BCD counter with JK flip-flops. (12)

15. (a) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are

$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$

$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$

$z = x_2 + y_1$

Draw the logic diagram of the circuit.

Derive the transition table and output map

Obtain a flow table for the circuit.

Or

(b) Show that dynamic hazards do not occur in two level AND-OR gate network.
