Reg. No. | | | | | | | | | | | | |

Question Paper Code : 91478

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Seventh/Eighth Semester

Electrical and Electronics Engineering

EI 2403/EI 73/10144 EC 605 —VLSI DESIGN

(Common to Instrumentation and Control Engineering/Electronics and Instrumentation Engineering)

(Regulation 2008/2010)

(Common to 10144 EC 605 —VLSI Design for B.E. (Part–Time) Seventh Semester EEE – Regulation 2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What do you mean by threshold voltage in enhancement mode?
2. Write the NMOS transistor current equation.
3. What is a stick diagram?
4. Give two properties of Bi CMOS inverter.
5. What is latch up condition?
6. What do you mean by regularity?
7. What is an FPGA?
8. What is a programmable logic device?
9. Write the VHDL code for a half adder.
10. What is a package in VHDL?

PART B — (5 × 16 = 80 marks)

11. (a) Compare and contrast enhancement mode and depletion mode MOSFET.

Or

(b) Discuss in detail the CMOS fabrication.

12. (a) Discuss in detail the NMOS and CMOS inverters.

Or

(b) Explain how to determine pull up to pull down ratio for an nMOS inverter driven by another nMOS inverter.

13. (a) Discuss about the following:

(i) Tally circuits

(ii) Dynamic CMOS and clocking. (16)

Or

(b) Explain the operation of a 4X4 barrel shifter.

14. (a) Explain the Design and operation of a Finite state machine PLA. (16)

Or

(b) Discuss the architecture of a PAL device and FPGA. (16)

15. (a) (i) Write the VHDL code to realize a 4 : 1 multiplexer and a JK flip flop. (8)

(ii) Write a VHDL code for a 4 bit parallel adder with test bench. (8)

Or

(b) Write the VHDL code to realize a 4 bit binary counter. (16)