Reg. No.: | | | | | | | | | | | | |

Question Paper Code : 91417

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64/10144 EC 704 — VLSI DESIGN

(Regulation 2008/2010)

(Common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant by body effect?

2. What is the need for design rules?

3. Give the expression for Elmore delay and state the various parameters associated with it.

4. List different types of scaling.

5. What is Complementary Pass Transistor logic? State its advantages over CVSL.

6. Differentiate Latch and Flip-flop.

7. What is a Tester, Test Fixture and Handler?

8. Mention the different types of CMOS testing techniques.

9. State the format for procedural assignment in verilog.

10. What is RTL modeling in Verilog.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Derive drain current of MOS device in different operating regions. (10)

(ii) Describe with neat diagram the well and channel formation in CMOS process. (6)

Or

(b) (i) Describe on CMOS process enhancements. (8)

(ii) With the processing steps involved, explain Copper dual damascene interconnect. (8)

12. (a) (i) Derive expressions for effective resistance and capacitance estimation using RC delay models. (8)

(ii) Discuss on transistor and interconnect scaling. (8)

Or

(b) (i) Derive the final expressions and explain path logical effort, path electrical effort, path effort and path branching effort. (8)

(ii) Size the transistors of CMOS three input NAND gate for logic ratio of $\frac{3}{1}$. (8)

13. (a) (i) Compare tatic and dynamic logic circuit with example. (8)

(ii) Explain the Dynamic and Static power reduction in low power design of VLSI circuits. (8)

Or

(b) (i) What are Klass semidynamic flip flops? Explain with their logic circuits. (8)

(ii) Discuss on skew tolerant Domino circuits. (8)

14. (a) (i) List the manufacturing test principles and explain them. (8)

(ii) Explain Built-in Self-Test. (8)

Or

(b) (i) Discuss on the Test Logic Architecture and Test Access Port. (8)

(ii) Explain on the scan design strategy of testing. (8)

15. (a) (i) Explain the verilog Gate Primitives along with their function maps. (8)

(ii) Write the verilog description for NAND latch with time delay of 2 units for each NAND gates. (8)

Or

(b) (i) Explain blocking and non-blocking assignments in Verilog with examples. (8)

(ii) Illustrate in verilog the construction of 4 input Multiplexer from three 2-input multiplexers. (8)
