Reg. No. : | | | | | | | | | | |

Question Paper Code: 43036

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Third Semester

Electrical and Electronics Engineering

14UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. In fundamental mode sequential circuits, inputs are

   (a) levels (b) pulses
   (c) both levels and pulses (d) none of these

2. What is the major advantage of ECL logic?

   (a) very high speed (b) wide range of operating voltage
   (c) very low cost (d) very high power

3. The output of an exclusive-NOR gate is 1. Which input combination is correct?

   (a) A=1, B=0 (b)A=0, B=1 (c) A=0, B=0 (d) none of these

4. The sum output of half adder is

   (a) sum = A exor B (b) sum = AB
   (c) sum = A + B (d) sum = A (ex-nor) B

5. How many flip flops are required to build a binary counter circuit to count from 0 to 1023?

   (a) 6 (b) 10 (c) 24 (d) 12

6. In the toggle mode a JK flip-flop has

(a) J = 0, K = 0 (b) J = 1, K = 1 (c) J = 0, K = 1 (d) J = 1, K = 0

7. Which of the following is a type of shift register counter?

(a) Decade (b) Binary (c) Ring (d) BCD

8. What programmable technology is used in FPGA devices?

(a) SRAM (b) FLASH (c) Antifuse (d) All of the above

9. How are the statements between BEGIN and END not evaluated in VHDL?

(a) Constantly (b) Simultaneously
(c) Concurrently (d) Sequentially

10. How many styles of modeling are there in VHDL?

(a) 2 (b) 4 (c) 3 (d) 1

PART - B (5 x 2 = 10 Marks)

11. State DeMorgan's theorem.

12. Draw a 1 to 2-demultiplexer circuit.

13. What are synchronous sequential circuit?

14. Define hazards and its types.

15. List the different types of 'operators' supported by VHDL.

PART - C (5 x 16 = 80 Marks)

16. (a) Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Determine the method of detecting the error using any one error detecting code. (16)

Or

(b) (i) Explain the basic working principles of ECL logic familes. (4)

(ii) Perform the following conversions:

(1) $1043_{10} = ?_2$

(2) $11011010_2 = ?_{10}$

(3) $11011010_2 = ?_8$

(4) $1111101011001110_2 = ?_{16}$

(5) $123_8 = ?_2$

(6) $ECE_{16} = ?_8$ (12)

17. (a) (i) Design a logic circuit to convert the Binary to Gray code. (8)

(ii) Implement a full subtractors using half subtractors. (8)

Or

(b) (i) Implement the function F(A, B, C, D) = Σ (1, 2, 5, 7, 9, 14) using MUX using different variable as selection variable. (8)

(ii) Simplify the following Boolean function in F(x, y, z, w) = ∑(0, 1, 2, 5, 8, 9, 10)

(1) sum of products form (SOP) (4)

(2) Product of sums form (POS). (4)

18. (a) Design BCD asynchronous counter with state table and state diagrams. (16)

Or

(b) Design a synchronous sequential circuit whose state diagram is shown in Figure 1.The type of flip-flop to be use is J-K…. (16)

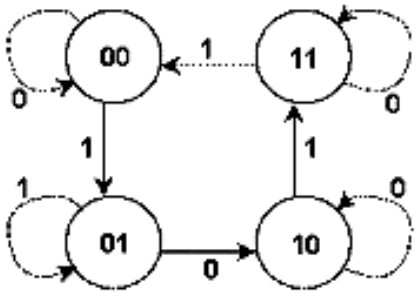

Figure 1

19. (a) Describe the steps involved in design of asynchronous sequential circuit in detail with an example. (16)

Or

(b) Develop the state diagram and state table for a logic system that has two input X and Y and one output Z, which is to behave in the following manner. Initially both input and output are equal to zero. Whenever $X = 1$ and $Y = 0$ the Z becomes 1. $X = 0$ and $Y = 1$ the Z becomes 0 $X = Y = 0$ or $X = Y = 1$ Z becomes no change. (16)

20. (a) Explain the structural VHDL description for a 2 to 4 decoder in details. (16)

Or

(b) Write a VHDL program and explain the design procedure of 4-bit comparator. (16)