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 **Reg. No. :**

**Question Paper Code: 43056**

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Third Semester

Electronics and Instrumentation Engineering

14UEI306 – DIGITAL ELECTRONICS

 (Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The three basic logic gates are

 (a) AND,OR and NOT gate (b) AND,OR and NOR (c) NAND, OR and NOT (d) None of the above

2. Solve 2’s complement subtraction of (010110 – 100101).

 (a) 0111 (b) 1111 (c) 1011 (d) 1110

3. The systematic reduction of logic circuits is accomplished by

 (a) Using Boolean algebra  (b) Symbolic reduction  (c) TTL logic (d) Using a truth table

4. A device that converts from octal to binary number is called

 (a) Decoder (b) Multiplexer (c) Encoder (d) De-multiplexer

5. D flip-flop during the occurrence of clock pulse if \_\_\_\_, the output \_\_\_\_ and if ­­­\_\_\_\_\_,

 the output is reset.

 (a) D = 0, Q = 0 , D is set (b) D = 1, Q = 1 , D = 0 (c) D = 1, Q is set , D = 0 (d) None of the above

6. ---------------------- is used for the purpose of detecting errors during transmission of binary information

 (a) Message bit (b) Carry bit (c) Parity bit (d) Selection bit

7. \_\_\_\_\_\_\_consists of a set of fixed AND gates connected to a decoder and a

 programmable OR array.

 (a) EPROM (b) EEPROM (c) PROM (d) EAPROM

8. For JK flip flop with J=1, K=0, the output after clock pulse will be \_\_\_\_\_\_\_\_

 (a) 0 (b) 1 (c) High Impedance (d) No change

9. PAL consists of a programmable \_\_\_\_ array and a fixed \_\_\_\_\_ array with output logic.

 (a) NAND and NOR (b) AND and NOR (c) NAND and OR (d) AND and OR

10. Flash memories are similar to

 (a) ROM (b) PROM (c) RAM (d) EEPROM

PART - B (5 x 2 = 10 Marks)

11. Obtain the canonical SOP form of the function Y=AB+ACD.

12. Define Multiplexer and draw its block diagram.

13. List out the applications of Flip Flops.

14. Define primitive flow table.

15. What is meant by PLA?

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Give a brief note on Weighted codes. (8)

 (ii) If ᾹB + CD̅ = 0 then. Prove that AB + C̅(A̅ + D̅) = AB + BD + B̅D̅ + A̅C̅D. (8)

Or

(b) Use Quine McClusky method to obtain the minimal sum for the following function. *F (X1 X2 X3 X4) = ∑* (0, 1, 3, 6, 7, 14, 15). (16)

17. (a) (i) Compare the characteristics of different Logic families. (8)

 (ii) Design a 4-bit Parallel Adder/Subtractor using logic gates. (8)

Or

(b) (i) Design a 2-bit magnitude comparator which *A1, A0* and *B1, B0*. (10)

 (ii) Implement full subtractor using demultiplexer. (6)

18. (a) Define Counter. Design a Synchronous decade counter using JK flip flop. (16)

Or

 (b) Explain the operation universal shift register with logic diagram. (16)

19. (a) Design an Asynchronous circuit that has two inputs x1 and x2 and output z. The

 circuit is required to give an output whenever the input sequence (0,0) (0,1) and

 (1,1) received but only in that order. (16)

Or

 (b) What do meant by hazards? Describe hazards in combinational and sequential

 circuits with suitable examples. (16)

20. (a) Explain about RAM and its types. (16)

Or

(b) (i) With a neat sketch, explain the block diagram of PLA. (8)

 (ii) Discuss in detail about EPROM and EEPROM. (8)