Reg. No. : | | | | | | | | | | |

Question Paper Code: 33056

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Third Semester

Electronics and Instrumentation Engineering

01UEI306 – DIGITAL ELECTRONICS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Convert the octal number 360.15 to decimal number.
2. State De-Morgan's theorem.
3. Draw the schematic of three input TTL NAND gate.
4. Suggest a solution to overcome the limitation on the speed of the adder.
5. How a D flipflop is converted into T flipflop.
6. Differentiate between edge triggering and level triggering.
7. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.
8. What is race conditions?
9. Define memory decoding.
10. Compare EPROM with EEPROM.

PART - B (5 x 16 = 80 Marks)

11. (a) Simplify the logic function F(A,B,C,D) = ∏(3, 5, 6, 11, 13, 14, 15) using K - map in SOP and POS form. (16)

Or

(b) Given Y (A, B, C, D) = ∏M (0, 1, 3, 5, 6, 7, 10, 14, 15), draw the K-map and obtain the simplified expression and realize using basic gates (16)

12. (a) Design a 3 bit binary to reflected code converter. Draw the logic diagram. (16)

Or

(b) Design a BCD to Excess-3 converter using truth table and k-map simplification. (16)

13. (a) Design a mod-7 synchronous binary counter using JK flip-flops. (16)

Or

(b) Design a sequence detector to detect the sequence "01110" using D Flipflops (one bit overlapping). (16)

14. (a) Give hazard free realization for the following Boolean function. F(A, B, C, D) = ∑m(0, 2, 6, 7, 8, 10, 12). (16)

Or

(b) Write short notes on races and hazards that occur in asynchronous circuits. (16)

15. (a) Implement the BCD to XS3 code conversion using ROM. (16)

Or

(b) Draw the block diagram of a PLA and explain its architecture. (16)

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