Reg. No. : | | | | | | | | | | |

Question Paper Code: 36044

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Sixth Semester

Electronics and Communication Engineering

01UEC604 - VLSI DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Define body effect.
2. List the various issues in Technology-CAD.
3. What is meant by crosstalk?
4. State the types of power dissipation.
5. Differentiate latch and flip-flop.
6. State any two criteria for low power logic design.
7. Name the different types of CMOS testing techniques.
8. What is mean by logic verification?
9. Write a verilog module for a half adder.
10. What are gate primitives?

PART - B (5 x 16 = 80 Marks)

11. (a) Explain in detail about ideal I-V characteristics and non-ideal characteristics of MOSFET. (16)

Or

(b) Illustrate the DC transfer characteristics of a CMOS inverter. (16)

12. (a) What is a BSIM model? Give its versions with SPICE levels. Mention the features of BSIM model. (16)

Or

(b) Discuss in detail about the resistive and capacitive delay estimation of the CMOS inverter circuit. (16)

13. (a) Compare the various logic circuit families. (16)

Or

(b) Explain in briefly about Synchronizers. (16)

14. (a) Explain the logic verification in various levels of abstraction. (16)

Or

(b) Explain the method of boundary scan test in detail. (16)

15. (a) Write a verilog HDL code for an 4 –bit ripple carry adder using structural model. (16)

Or

(b) Explain behavioral and gate level modeling with suitable example. (16)

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