|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |

**Reg. No. :**

**Question Paper Code: 52028**

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Second Semester

Computer science and Engineering

15UCS208 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. How many bits are required to represent the decimal numbers in the range 0 to 999 using straight binary code

(a) 8 (b) 10 (c) 12 (d) 16

2. Excess-3 code is known as

(a) Weighted Code (b) Cyclic redundancy Code (c) Self – Complementing Code (d) Algebraic Code

3. The type of memory used for storing boot instructions is

(a) Static RAM (b) Dynamic RAM (c) ROM (d) PLA

4. For JK flip Flop with J=1, K=0, the output after clock pulse will be

(a) 0 (b) 1 (c) high impedance (d) No change

5. In PAL, how 10L8 is represented

(a) 10-I/P L-Active Low Output 8 Outputs (b) 10-I/P L-Active Low Input 8 Outputs (c) 10-I/P L-Active Low Input Output 8 Outputs (d) none of these

PART - B (5 x 3 = 15 Marks)

6. Realize XOR gate using only NAND gates.

7. Convert the gray code numbers, 1010 and 0110 to binary numbers.

8. How to design 3-to-8 line decoder using 2-to-4 line decoders?

9. What is an excitation table?

10. List the types of asynchronous sequential circuits.

PART - C (5 x 16 = 80 Marks)

11. (a) Simplify the following Boolean function by using the Quine–McClusky Method:  
 . (16)

Or

(b) Minimize the following Boolean expression using Boolean identities F(A, B, C)=A′B+BC′+BC+AB′C′. (16)

12. (a) Explain Logical Implementation of Full – adder and Full – Subtractor. (16)

Or

(b) Design a 4 bit magnitude comparator with a neat sketch. (16)

13. (a) Implement the combinational circuit with a PLA having 3 inputs, 4 product terms and 2 outputs for the functions F1 = ∑m(3, 5, 6, 7), F2 = ∑m(0, 2, 4, 7). (16)

Or

(b) Design BCD to excess 3 code converter using PAL. (16)

14. (a) Design MOD 8 up/down counter using T- flip flops with necessary diagrams and tables. (16)

Or

(b) Realize a SR flip flop using NAND gates and explain its operation. (16)

15.(a) (i) What is the objective of state assignment in asynchronous circuit? Explain race

free state assignment with an example. (8)

(ii) Discuss about static, dynamic and essential hazards in asynchronous sequential circuits. (8)

Or

(b) Write short notes on races and cycles that occur in fundamental mode circuits. (16)