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 **Reg. No. :**

**Question Paper Code: 42027**

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Second Semester

Computer Science and Engineering

14UCS207 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

 (Common to Information Technology)

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. Convert 101012 to decimal

 (a) 16 (b) 21 (c) 19 (d) 20

2. When used with an IC, what does the term "QUAD" indicate?

 (a) 4 circuits (b) 2 circuits (c) 8 circuits (d) 6 circuits

3. Which of the following expressions is in the sum-of-products (SOP) form?

 (a) AB + CD (b) AB(CD) (c) (A + B)(C + D) (d) (A)B(CD)

4. Half adder

 (a) performs the addition of two bits (b) performs the addition of three bits (c) performs the addition of two bytes (d) performs the addition of three bytes

5. Boolean algebra is also known as

 (a) Gate algebra (b) Transistor algebra (c) Switching algebra (d) Counting algebra

6. 3 bits full adder contains

 (a) 3 combinational inputs (b) 4 combinational inputs

 (c) 6 combinational inputs (d) 8 combinational inputs

7. HDL stands for

 (a) Hardware Description Language(b) Hardware Design Language (c) High Design Language (d)High Description Language

8. For which of the following flip-flop the output clearly defined for all combinations of two inputs?

 (a) Q type flip-flop (b) R S type flip-flop (c) J K flip-flop (d) T flip-flop

9. Combinations that are not listed for input variables are

 (a) overflows (b) carry (c) dont cares (d) zero bits

10. In synchronous circuits-state assignments are made with the objective of

 (a) avoiding critical races (b) circuit reduction (c) both (a) and (b) (d) none of the above

PART - B (5 x 2 = 10 Marks)

11. Express the function Y =A+BCin canonical POS.

12. Explain the design procedure for combinational circuits.

13. Give the applications of Demultiplexer.

14. Define race around condition.

15. What is a state equation?

PART - C (5 x 16 = 80 Marks)

16. (a) Show that the dual of the exclusive-OR is equal to its complement.

Or

(b) How would you express the Boolean function using K-map and draw the logic diagram F(w,x,y,z)= ∑*m*(0,1,2,4,5,6,8,9,12,13,14) (16)

 17. (a) Explain in detail a binary multiplier. (16)

Or

(b) (i) Design a 4-bit magnitude comparator with neat diagram. (12)

 (ii) List the features of HDL language. (4)

18. (a) Explain Multiplexers in detail. (16)

Or

(b) (i) How would you design a 3:8 decoder using basic gates? (8)

 (ii) Deduce the design of a 1:4 Demultiplexer circuit. (8)

19. (a) (i) Construct and explain the working of a 4-bit Up/Down ripple counter. (8)

 (ii) Model a synchronous MOD-5 counter and explain with waveforms. (8)

 Or

 (b) A sequential circuit has two flip flops (A and B), two inputs (x and y) and an output (Z).

The flip flop input functions and the circuit output function are as follows.

JA = XB + y’B KA = xy’B’

JB = xA’ KB = xy’ + A

Z = xyA + x’y’B

 Obtain the logic diagram; sate table, state diagram and state equations. (16)

20. (a) (i) What is a Hazard? Give hazard free realization for the following Boolean function. F (A, B, C, D) = Σ m(0, 2, 6, 7, 8, 10, 12). (8)

 (ii) Find the ASM chart for binary multiplier. (8)

 Or

 (b) Write note on ASM chart. (16)