Reg. No. : | | | | | | | | | | |

Question Paper Code: 52971

M.E. DEGREE EXAMINATION, DECEMBER 2015

Elective

VLSI Design

15PVL504 – PHYSICAL DESIGN OF VLSI CIRCUITS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(5 x 20 = 100 Marks)

1. (a) (i) Explain layout rules in the design of VLSI circuits with neat sketches. (10)

(ii) Explain the layout of standard cell gate arrays. (10)

Or

(b) (i) Describe the layout of FPGA with an example. (10)

(ii) Write about the efficient algorithmic techniques used for VLSI layout. (10)

2. (a) (i) Design an algorithm for transforming a hiper graph into a graph. Discuss the effectiveness of your technique as it applies to the bipartition problem. (10)

(ii) Describe the Rectangular dual floor planning . (10)

Or

(b) (i) Prove that there is a one to one correspondence between sliceable floor plan and a normalized polish expression. (10)

(ii) Discuss on regular and linear placement. (10)

3. (a) Explain sequential and hierarchical approaches in Global routing. (20)

Or

(b) Example channel routing with example. State its advantages. (20)

4. (a) Explain in detail the zero stack algorithm with example. (20)

Or

(b) (i) Design an algorithm with bounded delay and small skew, using the linear delay model. (10)

(ii) With neat sketches explain unconstrained via minimization problem. (10)

5. (a) Explain the following

(i) Plan subset problem. (10)

(ii) OTC Routing. (10)

Or

(b) (i) List all possible routing requirements for Multiple Chip Module (MCM). (10)

(ii) Discuss about Programmable Logic Arrays. (10)