Reg. No. : | | | | | | | | | | |

Question Paper Code: 52173

M.E. DEGREE EXAMINATION, DECEMBER 2015

First Semester

VLSI Design

15PVL103 – VLSI DESIGN TECHNIQUES

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(5 x 20 = 100 Marks)

1. (a) (i) Explain operation of enhancement mode nMOS transistor. (8)

(ii) Explain in detail about the second order effects in the MOS transistors. (12)

Or

(b) (i) Discuss the small signal model of an MOS transistor. (10)

(ii) Explain the steps involved in the n-well CMOS fabrication process with necessary diagrams. (10)

2. (a) (i) Draw and explain the complementary CMOS inverter DC characteristics with necessary expressions. (12)

(ii) Determine pull up to pull down ratio for nMOS inverter driven through one or more pass transistors (8)

Or

(b) (i) Analyze the CMOS inverter with driving large capacitance loads. (10)

(ii) What is meant by transmission gate? List the applications of transmission gates and design a 2 x 1 multiplexer operation circuit using transmission gates. (10)

3. (a) (i) Explain about capacitance estimation of RC network present in CMOS circuits with relevant equation. (16)

(ii) Write short notes on transistor sizing. (4)

Or

(b) Explain all types of power dissipation in CMOS circuits with relevant equation. (20)

4. (a) (i) Explain with neat diagram the design of 4:1 multiplexer. (8)

(ii) Explain about the design of priority encoder. (8)

(iii) Write short notes on cross talk. (4)

Or

(b) (i) List the advantage of carry look ahead adder and explain its operation with neat diagram. (10)

(ii) Explain in detail about the architecture design for multipliers. (10)

5. (a) (i) Explain the hierarchical modeling concepts in digital design. (8)

(ii) Write a verilog HDL code for 4 bit ripple carry adder using gate level modeling. (8)

(iii) Write a brief note on the conditional statements available in verilog HDL. (4)

Or

(b) (i) What is test bench? (2)

(ii) Write a verilog program for 3 to 8 decoder in behavioral modeling. (8)

(iii) With all types of modeling, write verilog program for 4 bit magnitude comparator. (10)

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