Reg. No. : | | | | | | | | | | |

Question Paper Code: 52972

M.E. DEGREE EXAMINATION, DECEMBER 2015

Elective

VLSI Design

15PVL519 – SYSTEM DESIGN USING FPGA

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(5 x 20 = 100 Marks)

1. (a) Give a detailed account of FPGA based system design. (20)

Or

(b) (i) Implement a 4-bit Binary Counter using sequential PAL devices. (10)

(ii) Compare the architectures of CPLD and FPGA. (10)

2. (a) (i) What are the basic elements of FPGA? Explain its general architecture. (12)

(ii) Discuss the basic concepts of Programmable Interconnects in brief. (8)

Or

(b) Explain in detail about the XC2000 series Logic Cell Arrays. (20)

3. (a) Write short notes on

(i) Design Entry (10)

(ii) Functional Simulation. (10)

Or

(b) Explain the concepts of timing simulation and implementation in FPGA design flow with suitable examples. (20)

4. (a) (i) Explain the Verilog Logic-Gate Modeling in detail. (12)

(ii) Compare and contrast top down approach with synchronous approach. (8)

Or

(b) Explain the design procedure to implement a 4-bit shift register in a top-down schematic-based design using synthesis tool Xilinx ISE. (20)

5. (a) Give a detailed account of faults in system design. (20)

Or

(b) Explain in detail about BIST and its basic concepts. (20)