Reg. No. : | | | | | | | | | | |

Question Paper Code: 31336

B.E. / B.Tech. DEGREE EXAMINATION, NOVEMBER 2015

Third Semester

Electrical and Electronics Engineering

01UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Determine $(377)_{10}$ in Octal and Hexa-Decimal equivalent.
2. Define propagation delay.
3. Give one application each for multiplexer and decoder.
4. Realize the logic expression $Y= (AB)' +A+ (B+C)'$ using NAND gates only.
5. Convert T flip flop to D flip flop.
6. What is a master-slave FF?
7. What is a deadlock conditions?
8. Mention the applications of PLA.
9. Write a VHDL code for 2x1 MUX.
10. Write HDL behavioral model of T flip flop.

PART - B (5 x 16 = 80 Marks)

11. (a) What is Hamming code? Discuss how the Hamming code is used to test and correct the error in the given word using suitable examples. (16)

Or

(b) (i) With circuit schematic, explain the operation of a two input TTL NAND gate with totem-pole output (10)

(ii) Compare totem pole and open collector outputs. (6)

12. (a) (i) Reduce the following using K-Map method. $F=\sum m\ (2, 3, 4, 6, 7, 9, 11, 13)$. (8)

(ii) Design a full adder using two half-adder and an OR gate. (8)

Or

(b) (i) Implement the following Boolean function using 8:1 MUX:
F(A, B, C, D)=∑m (0, 1, 3, 4, 8, 9, 15). (10)

(ii) Design a code converter that converts a BCD to Excess-3 code. (6)

13. (a) (i) Explain the operation of a master slave JK flip flop. (8)

(ii) Design a 3 bit counter using T flip flop. (8)

Or

(b) Design a sequential circuit for the following state equations: $A(t+1)=C+D;\ B(t+1)=A;\ C(t+1)=B;\ D(t+1)=C$. (16)

14. (a) Design an asynchronous sequential circuit that has 2 inputs x_2 and x_1, and one output z. The output is to remain 0 as long as an x_1 is 0. The first change in x_2 that occurs while x_1 is 1 will cause z to be 1. z is to remain 1 until x_1 returns to 0. Construct a state diagram and flow table. Determine the output equations. (16)

Or

(b) (i) A combinational logic circuit is defined by the following function $f_1(a, b, c) = \sum(0, 1, 6, 7)$, $f_2(a, b, c) = \sum(2, 3, 5, 7)$ Implement the circuit with a PAL having three inputs, product terms and two outputs. (10)

(ii) Describe the concept and working of FPGA. (6)

15. (a) (i) Construct a VHDL module for a JK flip-flop. (8)

(ii) Express how arithmetic and logic operations are expressed using RTL. (8)

Or

(b) Write the VHDL code to realize a 3-bit Gray code counter using case statement. (16)