Reg. No.	:	
----------	---	--

Question Paper Code: 41342

B.E. / B.Tech. DEGREE EXAMINATION, NOVEMBER 2015

Third Semester

Electronics and Communication Engineering

14UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The equivalent hexadecimal of binary number 1011101.1011 is

	(a) B33	(b) EFF2.F	(c) 5 D.B	(d) 4A.67
--	---------	------------	-----------	-----------

2. Universal gates are

(a) NAND	and AND gates	(b) NOR and OR gates
(c) NAND	and NOR gates	(d) AND and OR gates

- 3. The logic required to decode the binary (1011) $_2$ by producing a HIGH indication on the output Y is
 - (a) $Y = \overline{D}C \ \overline{B}\overline{A}$ (b) $Y = D\overline{C} \ BA$ (c) $DC \ BA$ (d) $\overline{D}\overline{C} \ \overline{B}\overline{A}$

4. A circuit with many inputs and only one output is called

- (a) de multiplexer (b) decoder (c) half adder (d) multiplexer
- 5. How many flip flops are required to construct a mod 128 counter
 - (a) 4 (b) 3 (c) 7 (d) 5
- 6. The output frequency of a decade counter that is clocked from a 50 KHZ signal is
 - (a) 5 KHz (b) 50 KHz (c) 50 Hz (d) 12.5 KHz

7. CMOS fan out depends on

(a) power dissipation	(b) propagation delay
(c) current	(d) noise margin

- 8. A fixed architecture logic device with programmable AND gates followed by fixed OR gates is
 - (a) PLA (b) PAL (c) PROM (d) RAM

9. A circuit which do not operate in synchronous with clock signal is

(a) Synchronous sequential circuits	(b) Asynchronous sequential circuits
(c) FPGA	(d) combinational circuits

- 10. A state machine which uses only Input actions, so that the output depends on the state and also on inputs, is called
 - (a) moore model (b) ROM (c) mealy model (d) combinational circuits

PART - B (
$$5 \times 2 = 10 \text{ Marks}$$
)

- 11. Differentiate multilevel and multi output gate network.
- 12. Draw the 4-bit binary divider.
- 13. State the drawbacks of RS flip flop.
- 14. How does a static RAM differ from dynamic RAM?
- 15. What arte advantages of merging process?

PART - C (
$$5 \times 16 = 80 \text{ Marks}$$
)

16. (a) Simplify the following expression using Quine Mccluskey method $f[w, x, y, z] = \sum (0, 2, 3, 5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$ Realize the minimized function using NOR gates only. (16)

Or

(b) (i) Realize the following function as Multilevel NAND –NAND gate and Multilevel NOR –NOR gate $F = \overline{A} B + B (C + D) + E\overline{F} (\overline{B} + \overline{D})$ (10)

	(ii) Prove that	
	(A+B+D) (A+B+D) (B + C+D) (A + C) (A + C+D) = A C D + A C D + B C	C D.
		(0)
17. (a)	(i) Describe the working of a full subtractor.	(8)
	(ii) Design 1 to 8 demultiplexer.	(8)
	Or	
(b)) Design 4 bit Binary to BCD code converter.	(16)
18. (a)) Explain synchronous decade counter using T flip flop.	(16)
	Or	
(b)) Write short notes on	
	(i) Sequence generator	(8)
	(ii) Ripple counter	(8)
19. (a)	(i) Implement the Boolean function using PLA $w(a, b, c) = \sum m(1, 2, 4, 6)$	(10)
	$x(a, b, c) = \sum m(0, 1, 6, 7)$	
	$y(a, b, c) = \sum m(2, 6)$	
	(ii) Explain the operation of two input CMOS NOR gate.	(6)
	Or	
(b)) Describe the operation of FPGA with its architecture.	(16)
20. (a)) (i) Develop VHDL code for 3 to 8 decoder.	(8)
	(ii) Explain the method to eliminate static hazard in an asynchronous circuit	with
	an example.	(8)
	Or	

(b) Design an asynchronous sequential circuit that has two inputs x_1 and x_2 and one output z. The output z = 1 if x_1 changes from 0 to 1, z = 0 if x_2 changes from 0 to 1 and z = 0 otherwise. Realize the circuit using D FF. (16)