Reg. No. : | | | | | | | | | | |

Question Paper Code: 42972

M.E. DEGREE EXAMINATION, NOVEMBER 2015

Elective

VLSI Design

14PVL508 – TESTING OF VLSI CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. Malfunction of the clock is a
   (a) Local fault (b) Logical fault (c) Distributed fault (d) failure

2. The reed-muller expansion technique can be used to realize any arbitrary n-variable Boolean function using
   (a) NAND and EX-OR gate only (b) AND and EX-OR gate only
   (c) AND and EX-NOR gate only (d) NAND and EX-NOR gate only

3. The ability to establish a specific signal value at each node in a circuit by setting value on the circuit input is
   (a) Controllability (b) Observability (c) Predictability (d) Accessibility

4. How many patterns need for testing the *n* input combinational circuit using exhaustive testing approach?
   (a) 2^{n+1} (b) 2^{n} (c) N (d) 2^{n-1}

5. Among the following which is extends an edge pin testing
   (a) Self checking (b) Guided probe testing
   (c) Effect cause analysis (d) Fault simulation

PART - B (5 x 3 = 15 Marks)

6. Justify fault f dominates the fault g in two (x, y) inputs and one (z) output NAND gate for the condition f be z s-a-0 and g be y s-a-1.

7. Find the Boolean difference with respect to X_3 for the function $F(X) = X_1X_2 + X_3X_4$.

8. How the controllability and observability is obtained using the test points?

9. Design 3 bit LFSR/2 bit SR pseudo exhaustive pattern generator.

10. How the testing and diagnosis process is done by the UUT Reduction?

PART - C (5 x 16 = 80 Marks)

11. (a) (i) How to detect and locate faults in any given digital systems. (10)

(ii) Explain the event driven simulation using flowchart. (6)

Or

(b) Analyze the different types of delay models with a neat sketch. (16)

12. (a) How the test pattern is generated in PODEM for the combinational logic circuits and illustrate with an example. (16)

Or

(b) How the test vectors are generated using D-algorithm for the combinational circuit and illustrate with an example. (16)

13. (a) Illustrate the three forms of generic scan based design. (16)

Or

(b) Describe the DFT approaches using adhoc design rules. (16)

14. (a) (i) Describe the circular BIST architecture. (8)

(ii) How the output response analyzed by signature analysis? (8)

Or

(b) Explain about embedded RAM and how the BIST will be implemented in embedded RAM. (16)

15. (a) Explain the system level diagnosis in detail. (16)

Or

(b) Illustrate the application of error detecting and error correcting codes. (16)