Reg. No. : | | | | | | | | | | |

Question Paper Code: 42232

M.E. DEGREE EXAMINATION, NOVEMBER 2015

Second Semester

Computer Science and Engineering

14PCS202 - MULTI CORE ARCHITECTURE

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. Instruction execution steps involved are

   (a) issue, execute, write, commit (b) issue, read, write, execute

   (c) issue, write, execute, schedule (d) execute, schedule, read, write

2. The performance of the distributed shared memory multiprocessors depends on the _____ factors.

   (a) cache size, process count, block size

   (b) miss, data write back, un cached state

   (c) cache size, miss rate and block size

   (d) shared state, read miss, write miss

3. Simultaneous multithreading (SMT) has the ability to _____

   (a) hide latencies (b) centralized instruction issue

   (c) thread level parallelism (d) hyper threading

4. Avoiding address translation during indexing of the cache is _____

   (a) hit time reduction technique (b) synonyms or aliases

   (c) context switching (d) trace caches

5. Average time to access a sector a sector of data is _____
   (a) average seek time + average rotational delay + transfer time
   (b) average latency + seek + delay time
   (c) average hit time + miss time + delay time
   (d) None of the above

PART - B (5 x 3 = 15 Marks)

6. How do you calculate the pipeline CPI?

7. What is called loop carried dependence?

8. What is distributed memory multiprocessor?

9. What is exponential back off?

10. State the methods for performance tuning.

PART - C (5 x 16 = 80 Marks)

11. (a) Describe SMT and CMP architecture, state their challenges and how they are addressed in implementation. (16)

Or

(b) How the performances are measured for multi core systems and what are the challenges? How these performances can be improved? Discuss. (16)

12. (a) Describe multistage interconnection networks and buses. How these support in multiprocessor issues? (16)

Or

(b) Explain the concept of synchronization and asynchronous issues in multiprocessor environment? How are they addressed and discuss? (16)

13. (a) Describe Intel multi core architecture. What are the challenges that were overcome? Illustrate. (16)

Or

(b) Compare IBM cell and GPGPV architecture. How different challenges are addressed in mulitcore architecture. (16)

14. (a) Describe memory optimization and protection, suitable for multi core environment. (16)

Or

(b) Explain the design of memory hierarchy suitable for multi core system environment. (16)

15. (a) What is MPI? How shared memory programming is implemented? Write the challenges. (16)

Or

(b) Write short notes on

(i) Performance tuning (8)

(ii) Multi core programming (8)
