Reg. No. : | | | | | | | | | | |

Question Paper Code: 31227

B.E. / B.Tech. DEGREE EXAMINATION, NOVEMBER 2015

Second Semester

Computer Science and Engineering

01UCS207 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is the decimal equivalent of the largest binary number that can be obtained with 16 bits?
2. Differentiate gray code and binary code.
3. List the logic gates used in the design of combinatorial circuits.
4. State the identities applicable for exclusive OR operation.
5. Name the different HDLs.
6. Sketch the ROM block diagram.
7. Draw the basic flip flop circuit using NOR gates.
8. Draw the block diagram of a sequential circuit.
9. State the use of asynchronous sequential circuit.
10. List the types of race condition.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) State the laws of Boolean algebra. (6)

(ii) For the expression $F= (CD+E) (A+B')$ write the procedure to obtain the multilevel NAND gate diagram. (10)

Or

(b) (i) For the Boolean function $F= xy'z+x'y'z+w'xy+wx'y+wxy$ illustrate the truth table. (6)

(ii) Draw the logic diagram using Boolean expression for the above mentioned function. (10)

12. (a) Show that a full-adder can be constructed with two half-subtractors and an OR gate. (16)

Or

(b) Design a combinatorial circuit with three inputs and six outputs. The output binary number should be the square of the input binary number. (16)

13. (a) Implement the function $F (a, b, c) = \Sigma (1, 2, 4, 5)$ with a multiplexer. (16)

Or

(b) Design a combinatorial circuit using ROM. (16)

14. (a) Design a 4-bit binary ripple counter using D flip-flops. (16)

Or

(b) Implement T flip flop using D flip flop and JK flip flop. (16)

15. (a) (i) Explain the steps for the design of asynchronous sequential circuit. (8)

(ii) Explain the state reduction and flow tables in asynchronous circuit. (8)

Or

(b) (i) Discuss about static, dynamic and essential hazards in asynchronous sequential circuits. (8)

(ii) Explain the race-free state assignment with an example. (8)
