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**Question Paper Code : 31430**

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Sixth Semester

Electronics and Instrumentation Engineering

EI 2353/EI 63/10133 EI 603 — DIGITAL SYSTEM DESIGN

(Regulation 2008/2010)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the TTL inverter circuit.
2. What happens when excess gate voltage is given to CMOS devices?
3. How does the architecture of PLA different from PROM?
4. What is FPGA? State its significances.
5. Differentiate volatile and non-volatile memory.
6. What is memory expansion?
7. What is the need of control waveforms in multiplexing displays?
8. Write down the types of flash memory.
9. What are the factors that determine the complexity of deriving the test of a circuit?
10. Why Ad Hoc design for testability technique is more preferred than other DFT techniques?

PART B — (5 × 16 = 80 marks)

11. (a) Design a full adder using CMOS and dynamic CMOS. Also discuss their performances in detail.

Or

- (b) With neat sketch explain the (i) TTL to CMOS (ii) CMOS to TTL interfacing.

12. (a) (i) A combinational circuit is defined by the functions  $F_1(A, B, C) = \Sigma m(3, 5, 6, 7)$ ,  $F_2(A, B, C) = \Sigma m(0, 2, 4, 7)$ . Implement the circuit using PLA. (8)
- (ii) Briefly describe the various functional blocks of any CPLD. (8)

Or

- (b) Generate the following Boolean functions with a PAL with 4 inputs and 4 outputs.

$$Y_3 = A' BC' D + A' BCD' + A' BCD + ABC' D$$

$$Y_2 = A' BCD' + A' BCD + ABCD$$

$$Y_1 = A' BC' + A' BC + AB' C + ABC'$$

$$Y_0 = ABCD$$

13. (a) (i) Draw the 6T cell SRAM and explain its operation. (8)
- (ii) Write a technical note on different types of ROM. (8)

Or

- (b) (i) Using ROM, design a combinational circuit which accepts 3 bit number and generates an output binary number equivalent to the square of input number. (8)
- (ii) Describe features of main and peripheral memories. (8)

14. (a) With suitable diagram, explain the operation of PRBS Generator.

Or

- (b) (i) Discuss about frequency counter and draw its control waveforms. (8)
- (ii) Explain the basic operation of a digital voltmeter. (8)

15. (a) (i) Describe the major concepts used in Ad Hoc DFT technique. (8)
- (ii) Briefly explain any two advanced scan concepts used for testing. (8)

Or

- (b) (i) Discuss the BIST scheme for PLD and CPLDs. (6)
- (ii) Plot the following PLA on the map. Identify the undetectable faults. Derive a minimal test set for all detectable faults. (10)

Inputs				Outputs	
$x_1$	$x_2$	$x_3$	$x_4$	$z_1$	$z_2$
1	2	0	1	1	0
2	0	1	1	1	0
1	1	0	2	1	1
0	1	1	0	0	1