LIB
16/11/13 AN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 31422

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Fourth Semester

Electronics and Instrumentation Engineering

EI 2253/EI 43/10133 EE 406/080300014 — DIGITAL LOGIC CIRCUITS

(Regulation 2008/2010)

(Common to PTEI 2253 — Digital Logic Circuits for B.E. (Part –Time) Second Semester Electronics and Instrumentation Engineering — Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What is hamming code?

2. What are reduntant prime Implicants?

3. How the decoder is used as a demultiplexer?

4. Implement the function $F = A \cdot B$ using NOR gates?

5. How many flip – flops are required to build a binary counter that counts from 0 to 128?

6. Why is state reduction necessary?

7. What is primitive flow table?

8. State advantages of totem pole output.

9. What is memory expansion?

10. Define cycle in asynchronous circuits.

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Convert the function $f(A,B,C) = (A + \overline{B} + C)(\overline{A} + B + \overline{C})$. into standard sum of product form. (5)

(ii) The Hamming code 101101101 is received. Correct it if any errors. There are four parity bits and odd parity is used. (5)

(iii) Convert the following:

(1) $(61.3)_{10} = (\ )_2$

(2) $(37.29)_{10} = (\ )_8$

(3) $(101011)_2$ to Gray code. (6)

Or

(b) Determine the essential prime implicants of the following function and verify using k–map $f = \Sigma m(3,4,5,7,9,13,14,15) + \Sigma d(0,1)$

12. (a) (i) Compare Serial and parallel Adder. (6)

(ii) Implement following multiple output function using decoder and logic gates.

$f_1(A,B,C) = \Sigma m(1,4,5,7)$

$f_2(A,B,C) = \pi M(2,3,6,7)$ (10)

Or

(b) (i) Construct a Binary to BCD code converter using full address. (10)

(ii) Design a combination logic circuit with 3 input variables that will produce a logic 1 output when more than one input variables are logic 1. (6)

13. (a) (i) Draw and explain the working of 4 bit $up/\overline{down}$ synchronous counter. (12)

(ii) Give the excitation table for T flipflop (4)

Or

(b) (i) Design a synchronous counter with states 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5,... using JK ff's. (12)

(ii) Explain the concept of Bidirectional shift Register. (4)

14. (a) Design a T flipflop from logic gates.

Or

(b) (i) An asynchronous sequential circuit is described by the following excitation and output function.

$$Y = x_1x_2 + (x_1 + x_2)y$$

$$Z = y$$

(1) Draw the logic diagram of the circuit.

(2) Derive the transition table and output map.

(3) Describe the behaviour of the circuit (10)

(ii) Write notes on shared row state assignment and one hot state assignment. (6)

15. (a) (i) Design a BCD to Excess – 3 code converter and implement using suitable PLA. (10)

(ii) Give the classification of semiconductor memory. (6)

Or

(b) (i) Draw and explain the circuit for tri–state TTL inverter. (10)

(ii) Give the characteristics of ECL family. (6)