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Question Paper Code : 13009

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Fourth/Fifth Semester

Electrical and Electronics Engineering

EC 1312 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering/
Instrumentation and Control Engineering)

(Regulation 2007)

Time : Three hours — Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define propagation delay of a gate.
2. Draw the basic circuit of RTL NOR gate.
3. State the application of half adder circuit in real time digital systems.
4. Draw the truth table and graphic symbol of universal gates.
5. Define demultiplexer.
6. What is parity checker?
7. Give the characteristic table and excitation table of R-S flip-flop.
8. Draw the block diagram of Moore state machine.
9. Define flow table.
10. What is race?

PART B — (5 × 16 = 80 marks)

11. (a) Explain the different types of output configuration of TTL gates.

Or

(b) (i) What is transmission gate? Draw its basic circuit. (4)

(ii) Implement 4 × 1 multiplexer with transmission gates and explain. (12)

12. (a) (i) Simplify the following Boolean function and draw the logic diagram using NAND gates. $F(A, B, C, D) = \Sigma(3, 7, 11, 13, 14, 15)$. (10)

(ii) Design a half subtractor circuit. (6)

Or

(b) Design a four bit combinational circuit that outputs the 2's complement of the input binary number.

13. (a) (i) Draw a PLA circuit to implement the following functions.

$F_1 = A'B + AC' + A'BC$; $F_2 (AC + AB + BC)'$. (10)

(ii) Distinguish PAL and PLA with suitable example. (6)

Or

(b) (i) Write the HDL dataflow description of 2 to 4 line decoder. (10)

(ii) Construct a 16 × 1 multiplexer with two 8 × 1 multiplexer and one 2 × 1 multiplexer. Use block diagrams. (6)

14. (a) Design a sequential circuit with two J-K flip-flops and one input x. When $x = 0$, the state of the flip-flops does not change. When $x = 1$, the state sequence is 01, 11, 01, 11 (1 – 3 – 1 – 3) and repeat. Provide suitable state diagram and table.

Or

(b) Explain with a neat sketch, the operation of Universal shift register and state its applications.

15. (a) Find a circuit that has no static hazards and implements the Boolean function $F(A, B, C, D) = \Sigma(0, 2, 6, 7, 8, 10, 12)$.

Or

(b) (i) Explain the difference between asynchronous and synchronous sequential circuits. (6)

(ii) Describe fundamental mode operation. (4)

(iii) Explain the difference between stable and unstable states. (6)