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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 31433

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Eighth Semester

Electrical and Electronics Engineering

EI 2403/EI 73 – VLSI DESIGN

(Common to Seventh Semester – Electronics and Instrumentation Engineering and Eighth Semester – Instrumentation and Control Engineering)

(Regulation 2008)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the second order effects of the MOSFET device?
2. List the factors which affect the threshold voltage of a MOS transistor.
3. Compare inverting and Non-inverting supper buffers.
4. State the significance of Lamda based rules.
5. Draw the dynamic CMOS circuit for XOR logic gate.
6. What is anti-fuse technique? Mention its significances.
7. Differentiate between PROM and PAL programmable logic devices.
8. Draw the Macrocell architecture of PLACE 16V8 and state its significances.
9. Write the behavioral VHDL code for a SR latch.
10. Write a structural VHDL code for a 4:1 MUX.

PART B — (5 × 16 = 80 marks)

11. (a) Explain the various steps involved in CMOS fabrication process for an inverter. (16)

Or

(b) (i) Derive the current equation of a MOS device. (10)

(ii) Draw and discuss the MOS transistor Model. (6)

12. (a) Design a digital BiCMOS circuit that implements the function $f = c.k.r + r.k.p.$

Or

(b) (i) Draw the stick diagram for a XOR gate. (6)

(ii) Discuss the transfer characteristics, output characteristics, Pull up – Pull down ratios, timing and fan-out consideration of a CMOS inverter. (10)

13. (a) Design a 8:1 Mux using Dynamic CMOS and Clocked CMOS, assess the efficiency of each implementation.

Or

(b) Design and draw the CMOS structure and layout diagram for a 4 bit barrel shifter.

14. (a) Implement the following function using PAL 16 R8. Use minimum no. of product terms to implement the expression.

$F_1(a, b, c, d) = \Sigma(1,5,7,9,14)$

$F_2(a, b, c, d) = \Sigma(0,4,8,14)$.

Or

(b) Discuss the significances and working flow of programmable IOB, switch matrix and Programmable logic blocks of any FPGA with neat diagrams.

15. (a) Write the behavioral and structural VHDL code and test bench program for a JK Flip flop.

Or

(b) Write a behavioral VHDL code and test bench program for a 4-bit synchronous gray code counter.
