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Question Paper Code : 33366

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Third Semester

Electronics and Communication Engineering

EC 1203/EC 1251 — ELECTRONIC CIRCUITS — I

(Common to B.E. (Part-Time) Second Semester, Regulation 2005)

(Regulation 2004/2007)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Determine the stability factor of the circuit shown in Figure.1.

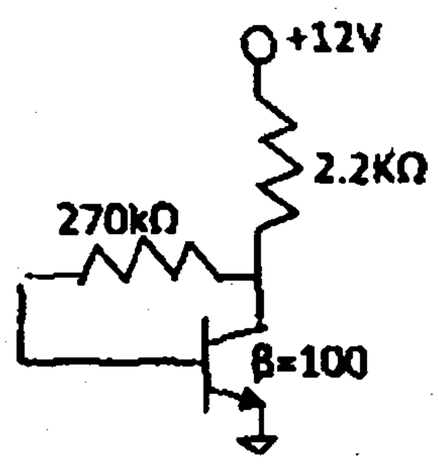

Figure 1

2. List out the advantages of self bias over other BJT biasing techniques.

3. Define CMRR. How to improve it.

4. Compare the characteristics of CS, CG and CD FET amplifiers

5. Draw the High-frequency hybrid-pi model of CE amplifier.

6. Define gain-bandwidth product.

7. Define Cross-Over distortion. How to eliminate it?

8. Compare between Class-A and Class-D amplifier.

9. Determine the rectification efficiency of half-wave rectifier.

10. A fill-wave rectifier using capacitor filter has to supply 30 V DC to a load resistance of 1 kΩ. Assuming the diode and transformer winding resistance to be negligible. Estimate for the value of capacitor filter for a ripple factor of 0.01.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Derive an expression to show the stability factor of voltage divider bias circuit. (6)

(ii) The circuit in Figure 2, let $\beta = 60$

(1) Find V_{TH} and R_{TH} for the base circuit

(2) Determine I_{CQ} and V_{ECQ}

(3) Draw the DC load line. (10)

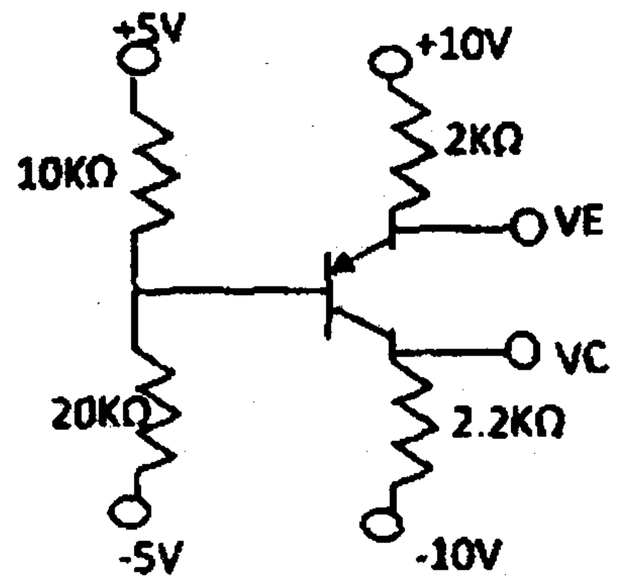

Figure 2

Or

(b) (i) Consider the circuit shown in Figure 3 with transistor parameters $I_{DSS} = 12\,mA, V_P = 3.5\,V$ and $\lambda = 0$. Let $R_1 + R_2 = 100\,k\Omega$ Design the circuit such that the DC drain current is $I_D = 5\,mA$ and the DC drain-to-source voltage is $V_{DS} = 5\,V$. (10)

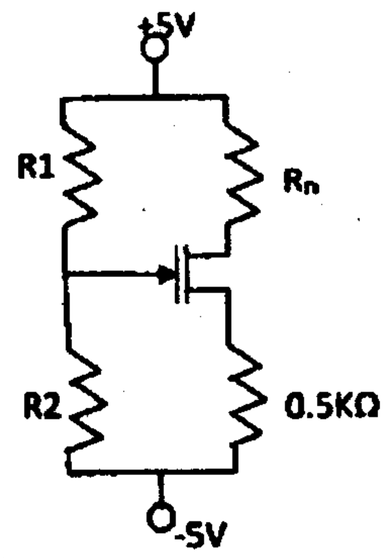

Figure 3

(ii) Discuss the use of JFET as a voltage variable resistor. (6)

12. (a) (i) For each transistor in the Darlington circuit shown in Figure 4 has the parameters of $\beta = 100, V_A = \infty$. Determine its overall voltage gain, input impedance and output impedance. (8)

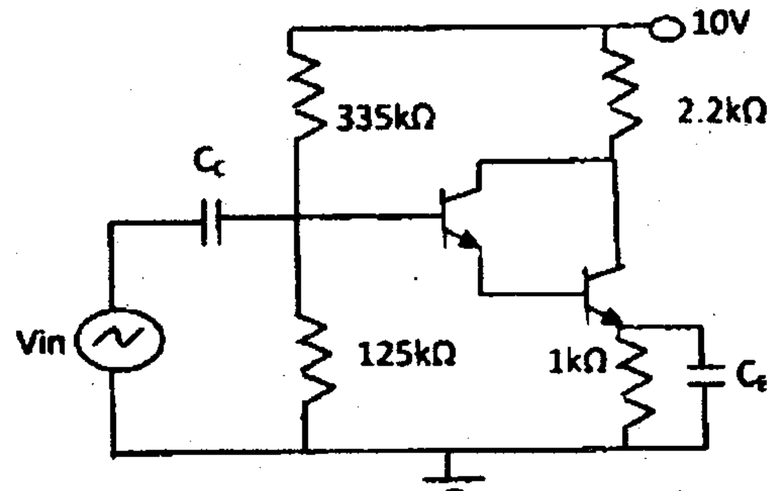

Figure 4

(ii) Determine the small signal voltage gain, input impedance and output impedance of common gate FET amplifier. (8)

Or

(b) For the circuit in Figure 5, the parameters are $R_B = 100\,k\Omega$, $R_E = 10\,k\Omega, R_C = 10\,k\Omega$, $V_{CC} = V_{EE} = 10\,V, R_L = 1\,k\Omega, R_s = 1k\Omega$ $\beta = 125$ and $V_A = \infty$

(i) Determine the small signal voltage gain (4)

(ii) Determine small signal current gain (4)

(iii) Determine the input resistance, Rin (4)

(iv) Determine the output resistance, Ro. (4)

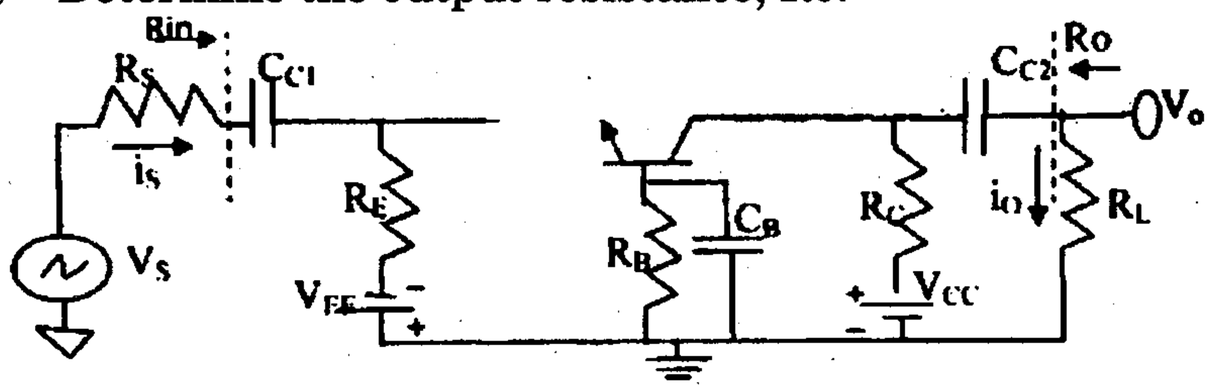

Figure 5

13. (a) (i) Determine the frequency response of multistage amplifier. (6)

(ii) Determine the midband gain, upper Cutoff frequency of a Common-Source amplifier fed with the signal having internal resistance Rsig = 100 kΩ (vide Figure 6). The amplifier has $R_G = 4.7\,M\Omega$, $R_D = R_L = 15\,k\Omega$, gm = 1 mA/V, ro = 150 kΩ, Cgs = 1pF and Cgd = 0.4 pF. (10)

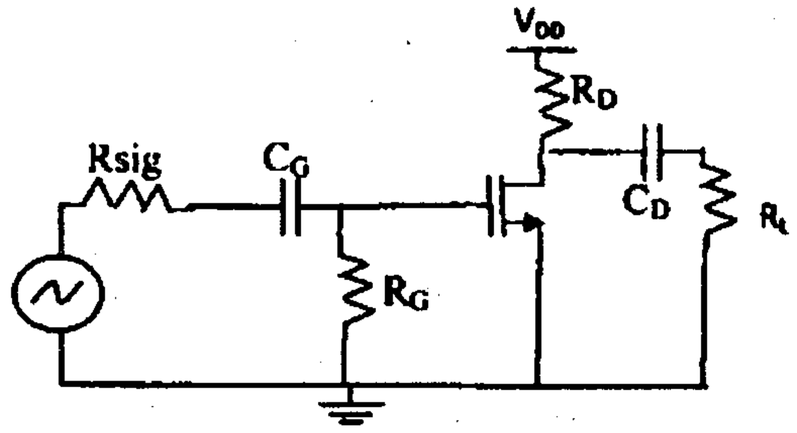

Figure 6

Or

(b) (i) Determine the mid-band gain and bandwidth of an CE amplifier (vide Figure 7). Assume lower cutoff frequency is 100Hz. (8)

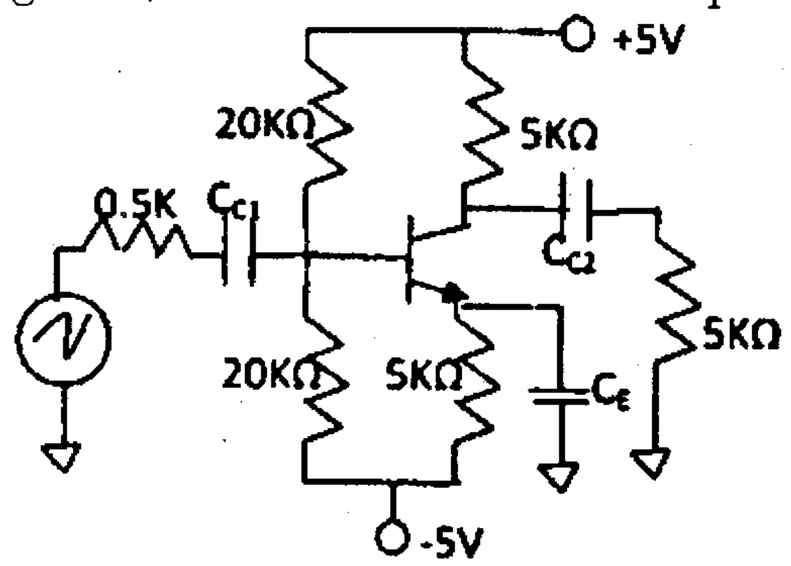

Figure 7

(ii) Find C_{C1}, C_{C2} and C_E. Let $\beta = 100$, cbe = 4pF, cbc = 0.2pF and $V_A = \infty$. (8)

14. (a) (i) Explain the transformer coupled Class-A amplifier in detail. (8)

(ii) Explain the Class-D amplifier in detail (8)

Or

(b) (i) Explain the Class-B complementary-symmetry push pull amplifier in detail. (8)

(ii) Determine the maximum power dissipation in a transistor and determine the temperature of the transistor case and heat sink. Consider a power MOSFET for which the thermal resistance parameters are $\theta_{dev-case} = 1.75^\circ$ C/W, $\theta_{case-sink} = 1^\circ$ C/W, $\theta_{sink-amb} = 5^\circ$ C/W and $\theta_{case-amb} = 50^\circ$ C/W. The ambient temperature is $T_{amb} = 30^\circ$C and the maximum junction or device temperature $T_{jmax} = T_{dev} = 150^\circ$C. (8)

15. (a) (i) Explain the working principle of SMPS in detail. (10)

(ii) Calculate the output voltage and zener current in the regulator circuit shown in figure 8. Let Vs = Vin = 15 V, Vz = 8.3 V and $\beta = 100$. (6)

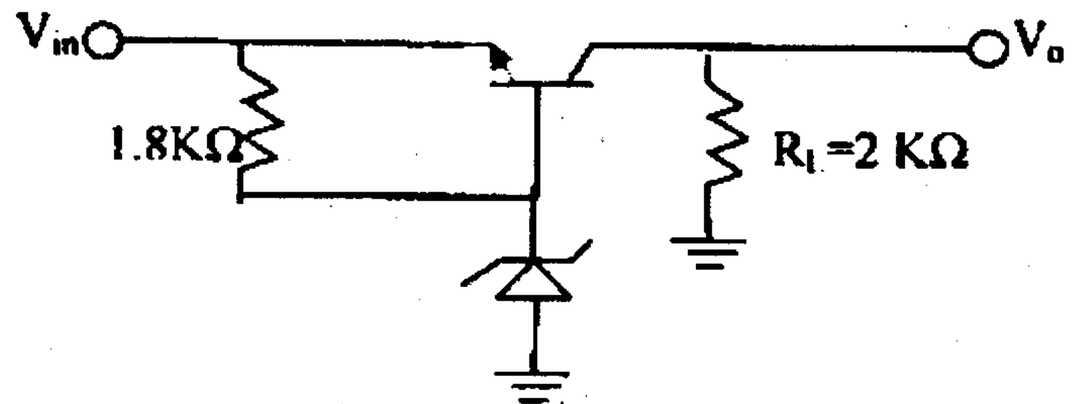

Figure 8

Or

(b) (i) Explain the power control using SCR in detail. (8)

(ii) Explain the C-L-C filter in detail. (8)