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Question Paper Code : 31373

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64/10144 EC 704 – VLSI DESIGN

(Regulation 2008/2010)

(Common to PTEC 2354 – VLSI Design for B.E.(Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare CMOS and BiCMOS technology.

2. Draw the DC transfer characteristics of CMOS inverter.

3. Define power dissipation.

4. Define scaling. Mention the types of scaling.

5. Implement a 2:1 Multiplexer using pass transistor.

6. Design a 1-bit dynamic register using pass transistor.

7. What is the need for testing?

8. What is the principle behind logic verification?

9. Differentiate blocking and non-blocking assignments.

10. Mention the possible values which are allowed in Verilog HDL.

PART B — (5 × 16 = 80 marks)

11. (a) Explain the electrical properties of MOS transistor in detail.

Or

(b) Derive an expression for V_{in} of a CMOS inverter to achieve the condition $V_{in} = V_{out}$. What should be the relation for $\beta_n = \beta_p$.

12. (a) Derive an expression for the rise time, fall time and propagation delay of a CMOS inverter.

Or

(b) Explain the various ways to minimize the static and dynamic power dissipation.

13. (a) (i) Implement $Y = (A + B)(C + D)$ using the standard CMOS logic. (8)

(ii) Implement NAND gate using pseudo-nMOS logic. (8)

Or

(b) (i) Implement D-flip-flop using transmission gate. (8)

(ii) Implement a 2-bit non-inverting dynamic shift register using pass transistor logic. (8)

14. (a) Describe in detail, the various manufacturing test in CMOS testing.

Or

(b) Explain in detail boundary scan testing.

15. (a) Write a Verilog HDL for an 8-bit Ripple Carry Adder using structural model.

Or

(b) Write a Verilog HDL for a positive edge-triggered D-flip-flop. Using that implement an 8-bit shift register in structural model.
